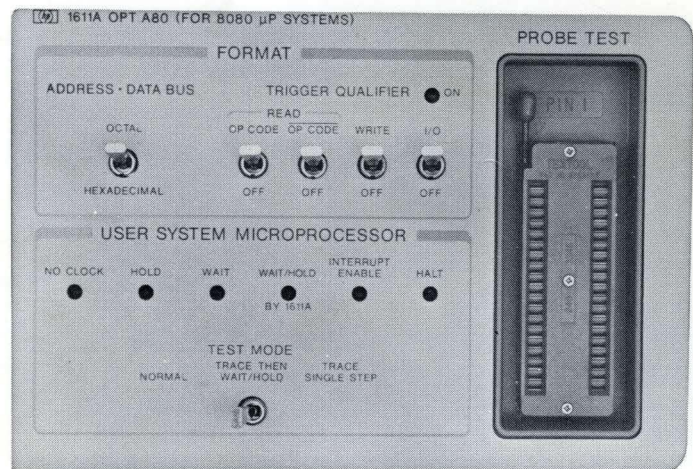


1611A OPT A80 (10258B) PERSONALITY MODULE FOR A80 MICROPROCESSORS



HEWLETT  PACKARD

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual, must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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OPERATING AND SERVICE MANUAL
SUPPLEMENT

**MODEL 1611A OPT A80
(10258B)
PERSONALITY MODULE
FOR
(A80 MICROPROCESSORS)**

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **1839A**.

With changes described in Section VII, this manual applies to instruments with serial numbers prefixed **1818A**.

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Manual Part Number 10258-90904
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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Manual Supplement contains: (1) information to install and test the Model 10258B; (2) operating information for the Model 1611A with Opt A80 installed; (3) service information that complements service data in Section VIII of the 1611A Operating and Service Manual.

1-3. DESCRIPTION.

1-4. The Hewlett-Packard Model 1611A Option A80 consists of an A80 Personality Module installed in a 1611A standard mainframe for use with microprocessor based systems which use the 8080 (or equivalent) microprocessor.

1-5. The Model 10258B is available as an accessory to provide the Model 1611A Logic State Analyzer with Option A80 capability.

1-6. SPECIFICATIONS.

1-7. Specifications for the Model 1611A with the Model 10258B installed are given in table 1-1.

1-8. RECOMMENDED TEST EQUIPMENT.

1-9. Equipment required to test the Model 10258B Option A80 and verify its operation is listed in table 1-2. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Model 1611A Specifications (Model 10258B Installed)

CLOCK (Φ_2 ONLY)

Repetition Rate: 300 kHz to 4 MHz.

Width: 75 ns minimum for either high or low state.

Threshold: 9 to 13 V, logic 1 (high); -1 to 0.8 V, logic 0 (low).

Input Resistance: approx 12 k Ω .

Input Capacitance: approx 25 pF, includes capacitance of 30.4 cm (12 in.) cable, approx 15 pF with 7.6 cm (3 in.) cable.

DATA, ADDRESS, WAIT, READY, HLDA, INTE, SYNC

Threshold: 3 V to 6 V, logic 1 (high); -1 to 0.8 V, logic 0 (low).

Input Resistance: approx 1 M Ω .

Input Capacitance: approx 25 pF, includes capacitance of 30.5 cm (12 in.) cable, approx 15 pF with 7.6 cm (3 in.) cable.

SETUP AND HOLD TIMES: timing measured at 8 V level for leading edge of Φ_2 and 1 V level for trailing edge.

Address and μP status on Data lines relative to leading edge of Φ_2 at T2.

Setup: 100 ns min.

Hold: 25 ns min.

Data relative to leading edge of Φ_2 at T3.

Setup: 100 ns min.

Hold: 25 ns min.

Sync relative to trailing edge of Φ_2 at T1.

Setup: 100 ns min.

Hold: 25 ns min.

Ready relative to trailing edge of Φ_2 at T2.

Setup: 80 ns min.

Hold: 0 ns min.

OUTPUTS: all timing relative to leading edge of Φ_2 in T3 cycle.

LOW: <0.4 V into 50 Ω .

HIGH: >2.0 V into 50 Ω (nominally 3.9 V into an open circuit).

READY OUTPUT: TTL open-collector compatible output capable of sinking at least 8 mA when active.

TRIGGER: duration, approx 75 ns (RZ format); delay, approx 350 ns after the Φ_2 clock pulse which defines a valid trigger.

TRACE POINT ($\sqcap$): provides a positive edge approx 350 ns after the Φ_2 clock that defines the specific valid trigger to be displayed on the 1611A. If the 1611A Delay is set so that trigger word is not displayed, Trace Point Output occurs approx 350 ns after the Φ_2 clock that defines the valid trigger word immediately preceding the first displayed word.

TRACE POINT ($\sqcap$): complement of Trace Point ($\sqcap$).

EXTERNAL PROBE INPUT

Resistance: approx 1 M Ω .

Capacitance: approx 25 pF measured at probe tip.

Threshold: 2.4 V to 5.5 V, logic 1 (high); -0.8 V to 0.8 V, logic 0 (low).

Setup Time: input must be present for at least 250 ns prior to leading edge at Φ_2 clock at T3.

Hold Time: input must be present for at least 0 ns after falling edge of Φ_2 clock at T3.

MICROPROCESSOR COMPATIBILITY

Intel: 8080, 8080A, 8080A-2, 8080A-1.

AMD: 9080A, 9080A-1, 9080A-2, 9080A-4.

NEC: μ PD8080, μ PD8080A-E.

TI: TMS8080, TMS8080A.

National: INS8080A.

NOTE

The 1611A Option A80 is designed to be compatible with any microprocessor that meets specifications of the Intel 8080A.

Table 1-2. Recommended Test Equipment

Instrument	Critical Specification	Recommended Model	Use*
Power Supply (1)		HP 6213A	P,T
Pulse Generators (2)	10 V output into 50 ohms, External trigger, 0 to +2.5 V DC offset, 0 to 1.4 μ s adjustable delay	HP 8013B	P
Digital Voltmeter	± 1000 Vdc range, 0.1% accuracy	HP 3465A	A,T
Dual Channel Oscilloscope	100 MHz BW min	HP 1740A	P,T
Logic State Analyzer	Pattern recognition and state display	HP 1600A	T
Logic Pulser	Pulse logic circuits	HP 10526T	T
Logic Probe	Monitor digital IC's	HP 10525T	T
50 Ω Feedthroughs (2)	50 Ω feedthrough termination	HP 10100C	P
BNC-to-alligator Clip Adapter (3)		HP Part No. 8120-1292	P
Current Tracer	1 mA to 1A sensitivity	HP 547A	T
Signature Analyzer		HP 5004A or ET 9254	T
* P=Performance Test; A=Adjustment; T=Troubleshooting			

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information and instructions for installing the Model 1611A Option A80 Personality Module.

2-3. Figures 2-1 and 2-2 are provided to facilitate component identification.

2-4. **MODULE INSTALLATION.** The 10258B consists of two printed circuit boards, an A80 Personality Panel, and the dedicated A80 Microprocessor Probe. To install the 10258B in an HP 1611A, proceed as follows:

- a. Set LINE switch to OFF position and disconnect power cord.
- b. Disconnect Microprocessor Probe A13 and External Probe A12 from rear panel.
- c. Loosen captive screw on rear of 1611A top cover. Remove top cover and disconnect ribbon cable A11W2 from A9 (see figure 2-1).
- d. Remove boards A5, A6, A7, A8, A9, and A10.
- e. Disconnect ribbon cable A11W1 from connector A1P2 on Main Board A1 (see figure 2-2).
- f. Remove screw that secures ground lug to A11 Board.
- g. Remove two mounting screws that secure the A11 Board to Keyboard Support MP27 and remove A11 from instrument.

h. Place Option A80 Personality Panel A11 in position and secure it with mounting screws removed in step g.

i. Secure ground lug to A11 as shown in figure 2-2.

CAUTION

Be sure that lug does not short to CRT mounting bracket.

j. Connect A11W1 into Main Board Connector A1P2 as shown in figure 2-2. Dot on main board indicates pin 1 of connector.

k. Install A10 Option A80 ROM Board and A9 Option A80 Personality Board onto Main Board A1 as shown in figure 2-1.

l. Connect A11W2 from Personality Panel to connector A9J1 on A9 board. Location of connector pin 1 is indicated by dot on board.

m. Reinstall A5, A6, A7 and A8 boards onto Main Board A1 as shown in figure 2-1.

n. Connect new Option A80 microprocessor probe A13 to A9 board through appropriate slot in rear panel and install two retaining screws.

o. Reconnect external probe A12 to A10 board through appropriate slot in rear panel and install two retaining screws.

p. Replace top cover to 1611A.

q. Reconnect power cord.

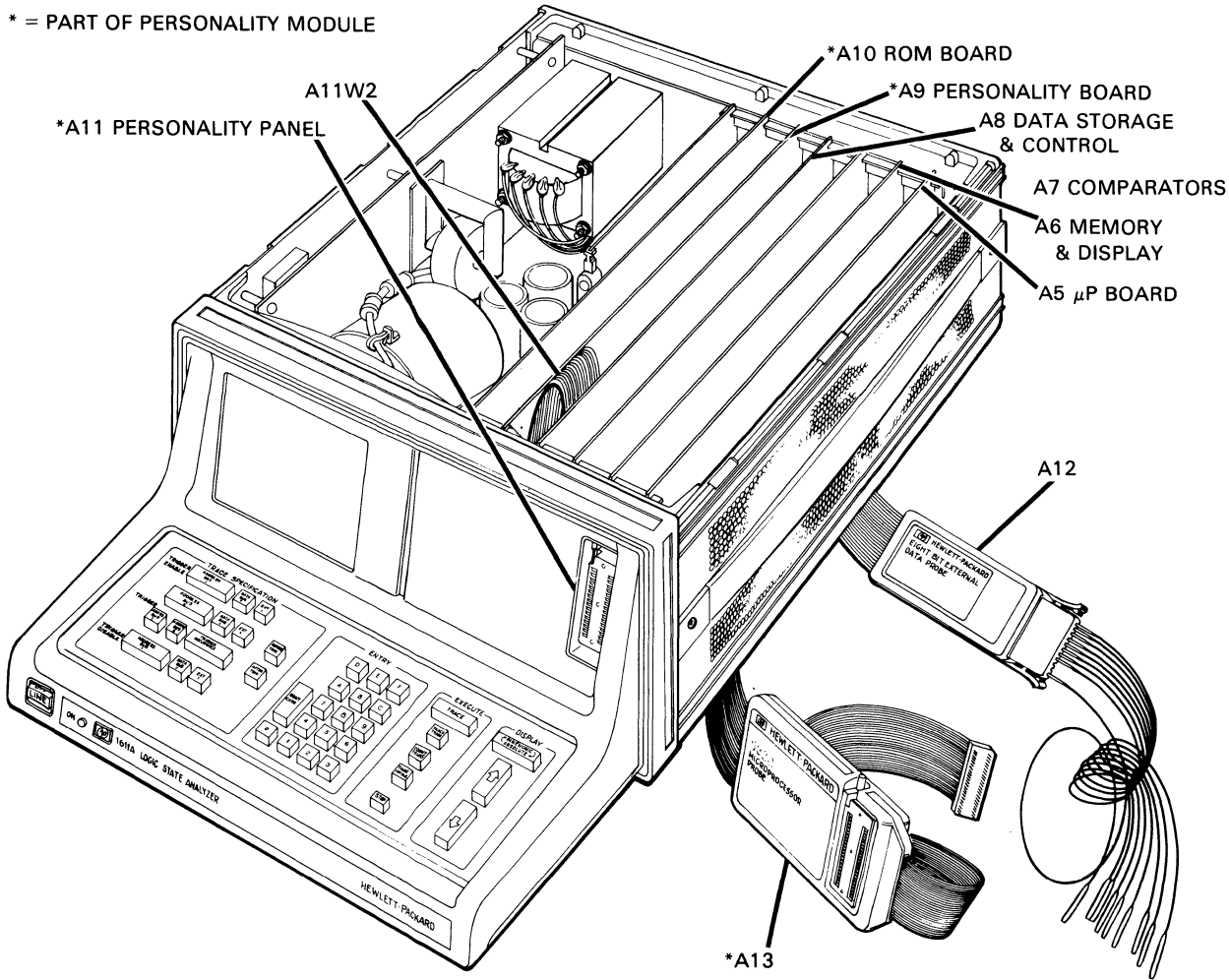


Figure 2-1. Model 1611A Assembly Locations

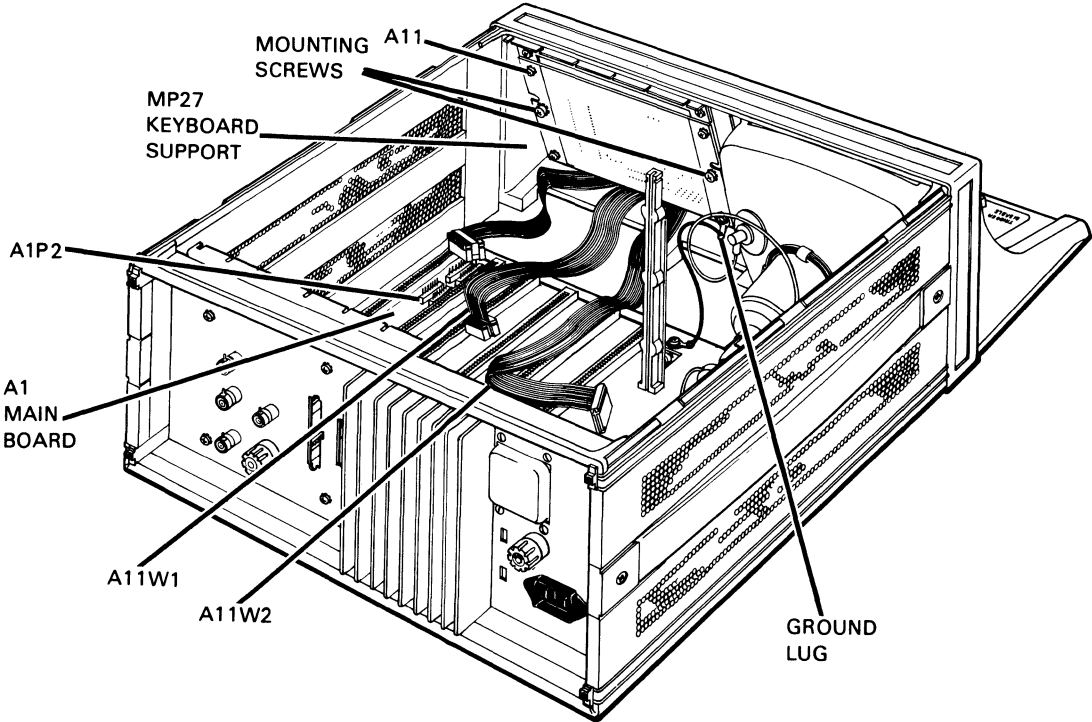
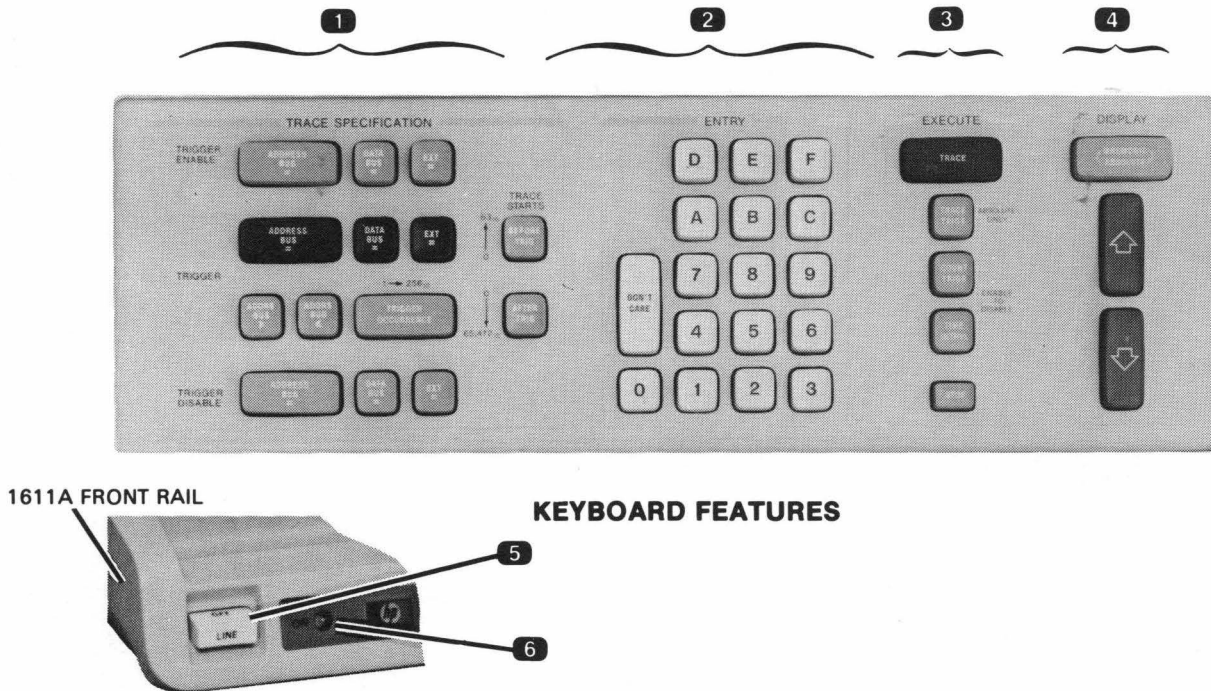


Figure 2-2. Personality Panel A11 Installation



1 TRACE SPECIFICATION GROUP. Controls for setting up trigger conditions.

TRIGGER Keys.

ADDRESS BUS =. Opens field for entry of desired program or memory address trigger word. Entry is made with up to four hex or six octal characters and is automatically right-justified with leading zeros assumed.

DATA BUS =. Permits selection of 8-bit trigger word on data bus. Entries may be made with up to two hex or three octal characters and are automatically right-justified with leading zeros assumed.

EXT =. Permits trigger selection on eight lines from External Probe A12. Entry is made in binary and is automatically right-justified with leading don't cares assumed.

ADRS BUS $\geq$ and ADRS BUS $\leq$. These keys permit triggering to be limited to activity $\geq$ or $\leq$ selected address. Entry is made with up to four hex or six octal characters and is automatically right-justified with leading zeros assumed.

TRIGGER OCCURRENCE. Used to determine the number of trigger word occurrences before the trace starts. Entries of a decimal number $1 \leq n \leq 256$ are allowed. Trigger Occurrence is used only in TRACE mode. (If no entry is made, field assumes a value of 1.)

TRIGGER ENABLE and TRIGGER DISABLE Keys. Allow trigger recognition only after Enable and before Disable specifications are met.

ADDRESS BUS =. Controls trigger enable (or disable) recognition on program or memory address word. Entry is made with up to four

hex or six octal characters and is automatically right-justified with leading zeros assumed.

DATA BUS =. Controls selection of an 8-bit trigger enable (or disable) word on data bus. Entries may be made with up to two hex or three octal characters and are automatically right-justified with leading zeros assumed.

EXT =. Controls trigger enable (or disable) recognition on eight lines from External Probe A12. Entry is made in binary and is automatically right-justified with leading don't cares assumed.

TRACE STARTS Keys. (TRACE mode only)

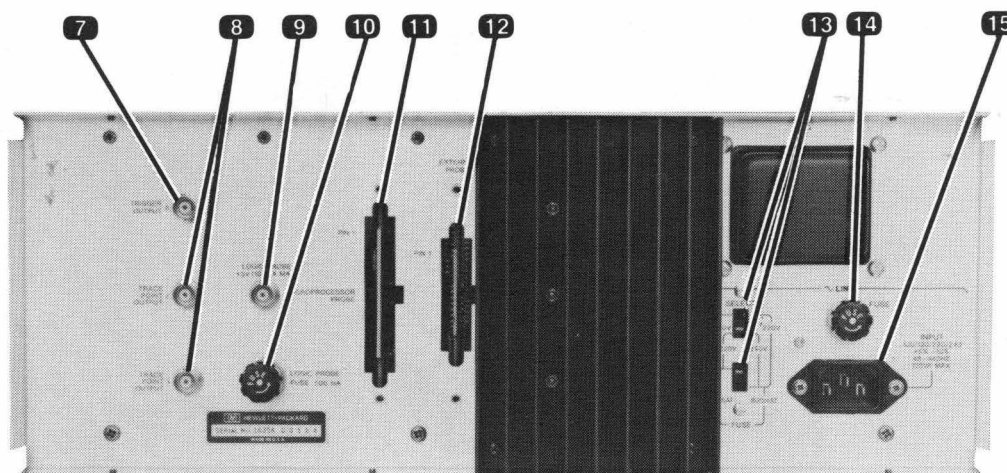
BEFORE TRIG. Selects number of memory transactions that trace starts before trigger (negative time or pretrigger). Entries are made with decimal number $n < 63$.

AFTER TRIG. Selects number of memory transactions that trace starts after trigger (delay). Entries may be made with decimal number $n \leq 65472$. If no entry is made via Before or After Trig, field assumes value of 0.

2 ENTRY GROUP. Alphanumeric keys and DON'T CARE key for entering data into open specification field. Keeping DON'T CARE key depressed approximately three seconds clears all TRACE SPECIFICATION entries. If no open data field at the time, the message NO OPEN DATA FIELD will flash until the clear is completed.

3 EXECUTE GROUP. Instructs 1611A to perform a specific task or measurement.

Figure 3-1.
Keyboard and Rear Panel Features
3-0



REAR PANEL FEATURES

TRACE. This mode provides for capture of 64 consecutive memory transactions in order to provide a display of microprocessor program execution.

TRACE TRIGGERS. In this mode, 1611A captures and displays only those memory transactions that match the preselected trigger conditions.

COUNT TRIGS. In this mode, 1611A counts trigger occurrences between Trig Enable and Trig Disable words.

TIME INTERVAL. This mode produces read-out of elapsed time between two states defined by Trigger Enable and Trigger Disable. Timing measurement is made using an internal 1 MHz clock; accuracy is $0.1\% \pm 1 \mu s$.

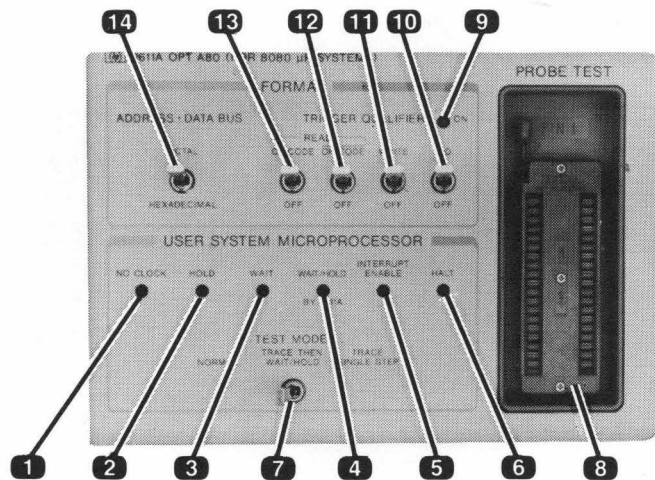
STOP. Halts any execute function in progress; display of activity of μP system under test immediately prior to STOP command will result and STOPPED message will be displayed

- 4 DISPLAY GROUP.** Used to control format of data displayed; keys do not change data stored in memory.

MNEMONIC/ABSOLUTE. Determines if data is displayed as captured (ABSOLUTE) or is to be inverse assembled into mnemonic statements with operands (MNEMONIC). In ABSOLUTE, each line of display represents one memory transaction which includes an address, data word, description of operation (e.g., op code, read, write), and eight external bits. In MNEMONIC, the data displayed often requires more than one memory transaction per line. The 1611A data display often contains less than 64 lines in MNEMONIC mode although data content is the same as in the 64-line ABSOLUTE display.

ROLL ↑ ↓. Used to roll 16-line display window through 64-byte memory.

- 5 LINE.** Line power switch.
- 6 ON.** Indicator lights when line power is on.
- 7 TRIGGER OUTPUT $\square$.** Provides ~ 75 ns, RZ, TTL output on each occurrence of selected trigger word (useful for triggering test equipment).
- 8 TRACE POINT OUTPUT ($\square$) ($\square$).** These outputs are levels which change state when a trace is initiated; they return to previous state when a trigger word is recognized or trace point is reached after delay. This provides a transition for triggering and a pulse for gating or causing breakpoints with external logic.
- 9 LOGIC PROBE.** +5 V power connector for logic probes requiring less than 100 mA.
- 10 LOGIC PROBE FUSE.** 500 mA fuse for Logic Probe Power.
- 11 MICROPROCESSOR PROBE.** Microprocessor Probe Connector.
- 12 EXTERNAL PROBE.** External Probe connector.
- 13 LINE SELECTOR.** Slide switches for selecting 100-, 120-, 220-, or 240-Vac line operation.
- 14 FUSE.** Use 1.0 AT time-delay fuse for 100-, 120-Vac operation; 800-mAT time-delay fuse for 220 or 240-Vac operation.
- 15 POWER INPUT.** Power cable connector.



- 1 NO CLOCK.** Light is on when no $\Phi 2$ clock from microprocessor under test is present or when $\Phi 2$ clock period is greater than approximately $7 \mu s$.
- 2 HOLD.** Indicates 8080 HLDA line is high and microprocessor is holding.
- 3 WAIT.** Indicates 8080 WAIT line is high.
- 4 WAIT/HOLD BY 1611A.** Indicates when wait or hold state is generated by 1611A in TRACE THEN WAIT/HOLD or TRACE SINGLE STEP mode. Wait state is generated when Probe A13 switch is in READY position. Hold state is generated when Probe switch is in HOLD position.
- 5 INTERRUPT ENABLE.** Indicates 8080 INTE line is high. Provides status of enable bit internal to microprocessor which allows interrupt to be processed.
- 6 HALT.** Indicates that a Halt instruction has been executed by 8080 and the microprocessor is halted.
- 7 TEST MODE.**

NORMAL. Data is captured and displayed with microprocessor under test operating without interruption of program flow.

TRACE THEN WAIT/HOLD. 1611A executes TRACE or TRACE TRIGS, and when data acquisition is completed, places microprocessor under test in Halt state.

TRACE SINGLE STEP. Only one instruction cycle is processed and displayed during each TRACE execution. 1611A halts microprocessor under test after each instruction cycle.
- 8 PROBE TEST.** Test socket for microprocessor probe; provides test pattern to Probe A13 for testing most system functions and controls.
- 9 TRIGGER QUALIFIER.** Indicates that Trace Specification (including TRIGGER, ENABLE, and DISABLE) must occur during a specific type of machine cycle before 1611A trigger will occur. When trigger requirements are satisfied via Trigger Qualifiers, a TRACE measurement proceeds normally (Before or After Trigger specification and data acquisition are not affected). If all switches are in OFF position, then the 1611A will trigger on any machine cycle that meets TRACE SPECIFICATION requirements.
- 10 I/O.** Allows 1611A trigger to occur only on Input/Output machine cycles.
- 11 WRITE.** Allows 1611A trigger to occur only on Memory Write machine cycles.
- 12 READ $\overline{OPCODE}$.** Allows 1611A trigger to occur only on Memory Read machine cycles other than Op-Codes.
- 13 READ OP CODE.** Allows 1611A trigger to occur only on Op-Code Fetch machine cycles.
- 14 OCTAL/HEXADECIMAL.** Selects octal or hexadecimal format for data display and Trace Specifications. Binary and decimal numbers are unaffected. Flashing ?(s) displayed in Trace Specification field(s) when the code entered is not complete enough for exact conversion to the other base (specification contains "don't care(s)" in least significant digit(s)).

NOTE

When Probe A13 switch is in HOLD position, the 8080 CPU must be in Probe A13 socket with Probe A13 connected to an energized user system for halting to be possible.

Figure 3-2. Personality Panel Controls and Indicators

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section provides operating information, explains functions of 1611A controls, connectors, and indicators, and describes measurement capabilities and operating characteristics of the 1611A with a Model 10258B Option A80 installed.

3-3. PANEL FEATURES.

3-4. Keyboard and rear-panel features are shown in figure 3-1. Personality Panel A11 is shown and described in figure 3-2.

3-5. **PROBES.** The 1611A uses two probes to acquire data from the system under test. Primary Probe A13 is dedicated to the microprocessor and is not interchangeable with other 1611A options. It gathers signals from the microprocessor Address and Data busses along with the clock and control signals. Connection is made from the probe pod to the microprocessor socket in the system under test through a ribbon cable and connector. The pod contains a socket for the microprocessor. If the microprocessor cannot be removed from the system, the connector cable and plug can be replaced with a ribbon cable terminated with a dual in-line clip connector which provides a direct connection from the pod to the microprocessor. When the clip is used, the socket on the probe pod is left empty.

3-6. The HOLD-READY switch on Probe A13 allows the 1611A to halt the μ P system under test two ways. Either the μ P Hold input or the μ P Ready input can be used to halt the μ P under test in TRACE THEN WAIT or TRACE SINGLE STEP mode.

3-7. When Probe A13 switch is in HOLD position, the 1611A can halt the μ P test only if the 8080 CPU is in Probe A13 socket and Probe A13 is connected to the user system. Halting is not possible if Probe A13 switch is in HOLD position and Probe A13 is connected to the 8080 CPU by the dual-in-line clip connector.

3-8. When Probe A13 switch is in READY position, the μ P system under test can be halted either with 8080 CPU in Probe A13 socket, or with Probe A13 connected to the 8080 CPU by the dual-in-line clip connector. The Ready output of Probe A13 is an open-collector TTL circuit that can sink at least 8 mA when active.

3-9. The external probe A12 is secondary, with no clock input, and is not required for instrument operation. It has eight uncommitted input lines to accept data coincident with data bus inputs on the primary probe. Input

impedance is approx 1 M Ω shunted by ≤ 25 pF at the probe tip.

3-10. SETTING TRACE SPECIFICATIONS.

3-11. At instrument turn on, the display should be as shown in figure 3-3. The display is divided into two parts by a dashed horizontal line. Above this line, all pertinent trace specifications are displayed as they are entered. The trigger ADDRESS bus field is open (inverse video field to right of TRIGGER). A blinking cursor in the lower left corner of the field indicates where a character entered by means of the ENTRY key group will be located.

3-12. The first step in making a measurement is to set up the trace specification. Pressing the key for the desired specification in the TRACE SPECIFICATION key group opens the data field. This field is now ready to accept data from the ENTRY key group for ADDRESS (Octal or Hex), DATA (Octal or Hex), or EXTERNAL (Binary only) specifications.

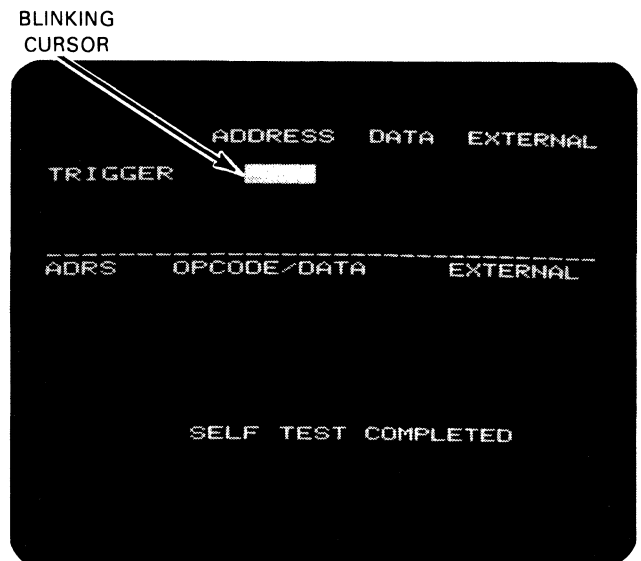


Figure 3-3. Turn-on Display

3-13. To enter data in the field, key in the desired value. If the pressed key is an illegal character for the selected specification field (such as an alpha character for a decimal field), an ILLEGAL CHARACTER message is flashed on the display. This message is cleared when the ENTRY key for an acceptable character is pressed, or when a new TRACE SPECIFICATION, EXECUTE, or DISPLAY field key is selected. All entries are automatically right-justified, and any EXTERNAL entries

automatically assume leading don't cares, while ADDRESS and DATA entries automatically assume leading zeros.

3-14. An existing trace specification can be changed or deleted in the following manner. To change a trace specification, press the TRACE SPECIFICATION key for that field, then enter the new data. To delete a trace specification, press the TRACE SPECIFICATION key for that field, then press DON'T CARE in the ENTRY key group. All TRACE SPECIFICATION fields can be "cleared" by pressing DON'T CARE key for approximately three seconds.

3-15. **TRIGGERING.** The TRIGGER keys ADDRESS BUS =, DATA BUS =, and EXT =, can be used in any combination to specify a 1611A trigger word. ADDRESS BUS = key allows 1611A to trigger on a desired μ P program or memory address word. DATA BUS = key allows 1611A to trigger on a desired μ P data bus word. EXT = key allows 1611A to trigger on a desired external word. When more than one key is used, all requirements must be satisfied. The TRIGGER ENABLE field allows the 1611A to recognize only those triggers which occur after the Enable specification has been detected. The TRIGGER DISABLE field allows the 1611A to recognize only those triggers which occur before the Disable specification has been detected. When used together, the Enable and Disable fields define a window, in which the 1611A is allowed to search for specified triggers. The ADDR BUS $\geq$ key allows any address bus value which is greater than or equal to the value specified (from the value specified up to $FFFF_{16}$ or 177777_8) to be recognized as a trigger. The ADDR BUS $\leq$ key allows any address bus value which is less than or equal to the value specified (from the value specified down 0000_{16} or 000000_8) to be recognized as a trigger. These two keys may be used together to define ranges over which any address bus activity will generate a trigger. For example, if a smaller number is entered in $\geq$ field than is entered in the $\leq$ field, then only the address bus activity within this window will be recognized. If a larger number is entered in $\geq$ field than is entered in the $\leq$ field, then the address bus activity which occurs outside of this window will be recognized and displayed. Trigger requirements, including Enable and Disable, can be restricted to particular μ P machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11.

3-16. TRACE MEASUREMENT EXECUTION.

3-17. **TRACE.** This is the most common mode of data acquisition. Trace mode allows capture of up to 64 consecutive memory transactions from the microprocessor system under test. After a completed Trace measurement run, the 1611A high-speed memory contains up to 64 memory transactions. The memory transactions are viewed through a 16-line movable window (figure 3-4). Thus, in Trace mode the 1611A can monitor and display the program execution of the microprocessor system under test.

3-18. The starting point for data acquisition is selected via the TRIGGER, TRIGGER OCCURRENCE, and

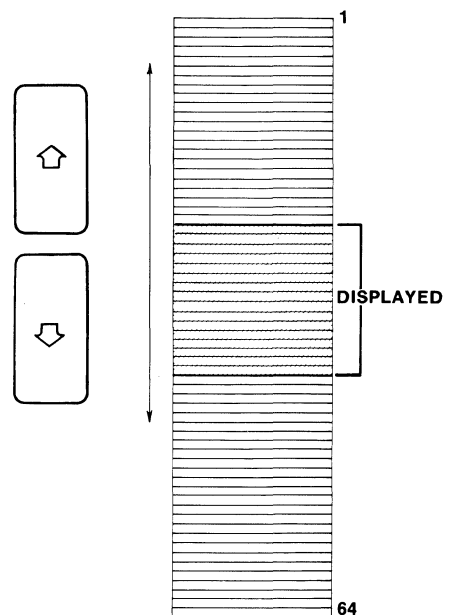


Figure 3-4. Display Window

BEFORE or AFTER TRIG Keys. The TRIGGER OCCURRENCE requirement will allow the 1611A to recognize the trigger only on the nth occurrence (with n being any desired value from 1 to 256; if no entry is made, field assumes a value of 1). The BEFORE TRIG Key can be used to start the trace up to 63 words before the trigger. This permits viewing of events leading up to the trigger (negative-time or pretrigger). The AFTER TRIG Key can be used to delay start of the trace up to 65 472 transactions after the Trigger event (figure 3-5). When AFTER TRIG delay is used, the data captured in high-speed memory will not contain the Trigger word.

3-19. Trace display may be viewed in ABSOLUTE or MNEMONIC mode. In both modes the program or memory address is displayed in the ADRS column. In ABSOLUTE (figure 3-6), the machine language op-code or data and the type of μ P machine cycle (e.g., READ), OPCODE, WRITE) are displayed in the OPCODE/DATA column (table 3-1). In MNEMONIC, the assembly language mnemonic and 8 or 16 bit operand (if the operand exists) are displayed in the OPCODE/DATA column (figure 3-7). If an invalid op-code is detected, then *** will be the flashing in the OPCODE/DATA column when in MNEMONIC MODE. IF *'s are displayed NOT flashing then the operand was not captured by high-speed memory. Single byte operand displays are ** (Hex) or *** (Octal). Two-byte operand displays are **** (Hex) or ***** (Octal). Hexadecimal or octal format can be selected and interchanged in both display modes.

3-20. Trace measurements may be made in NORMAL, TRACE THEN HALT, or TRACE SINGLE STEP mode. These modes are selected by the TEST MODE switch on Personality Panel A11. In NORMAL, the 1611A captures and displays data while the microprocessor system under test operates without interruption of program flow. In TRACE THEN HALT, the 1611A places the μ P

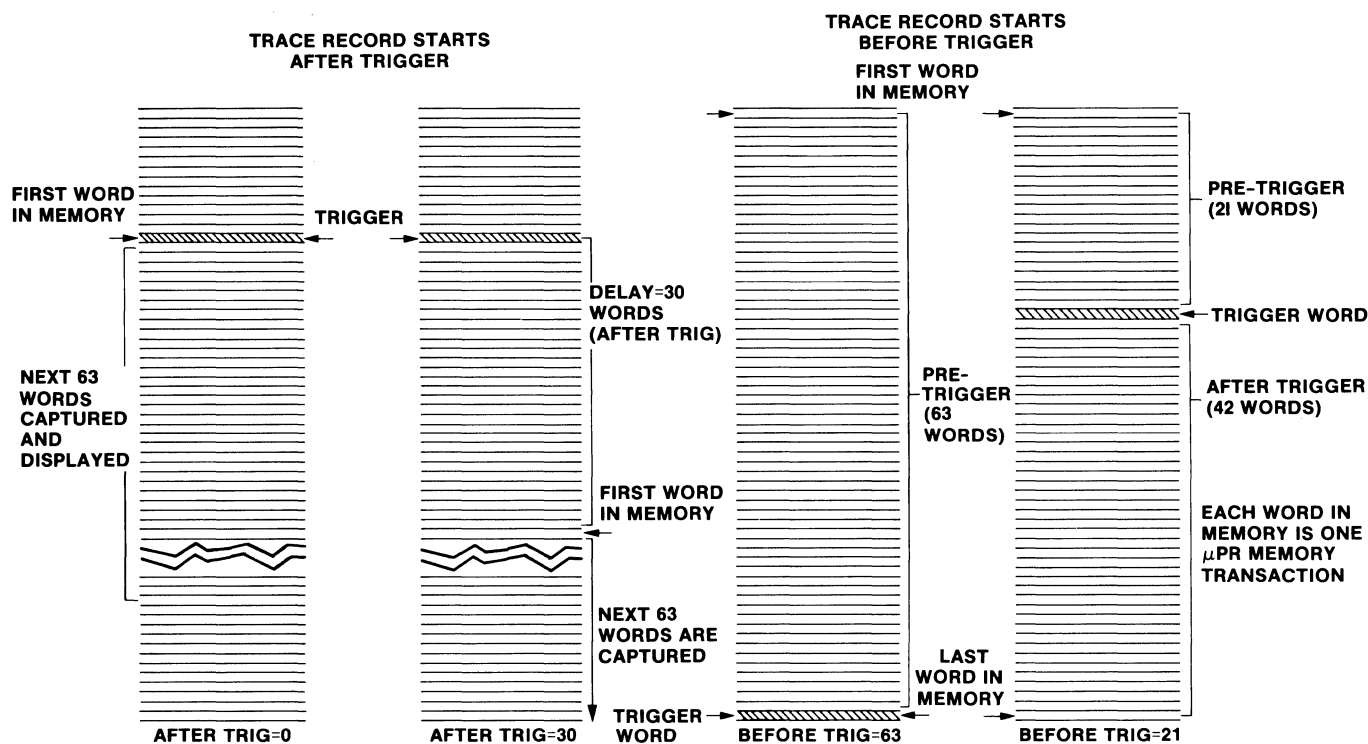


Figure 3-5. After Trigger and Before Trigger Displays

ADDRESS DATA EXTERNAL				
TRIGGER 0000				
ADDRESS			DATA	EXTERNAL
0000			00	WRITE
0000	00	WRITE	0000	0000
1111	11	OUTPUT	0000	0000
2222	22	OPCODE	0000	0000
3333	33	INPUT	0000	0000
4444	44	OUTPUT	0000	0000
5555	55	OUTPUT	0000	0000
6666	66	INPUT	0000	0000
7777	77	INPUT	0000	0000
8888	88	WRITE	0000	0000
9999	99	OUTPUT	0000	0000
AAAA	AA	OPCODE	0000	0000
BBBB	BB	INPUT	0000	0000
CCCC	CC	OUTPUT	0000	0000
DDDD	DD	OUTPUT	0000	0000
EEEE	EE	INPUT	0000	0000
FFFF	FF	INPUT	0000	0000

Figure 3-6. Absolute Mode Display

ADDRESS DATA EXTERNAL				
TRIGGER 0000				
ADDRESS			DATA	EXTERNAL
0000			00	WRITE
0000	00	WRITE	0000	0000
1111	11	OUTPUT	0000	0000
2222	22	SHLD ****	0000	0000
3333	33	INX SP	0000	0000
4444	44	OUTPUT	0000	0000
5555	55	OUTPUT	0000	0000
6666	66	MOV H,M	0000	0000
7777	77	MOV M,A	0000	0000
8888	88	WRITE	0000	0000
9999	99	OUTPUT	0000	0000
AAAA	AA	XRA D	0000	0000
BBBB	BB	CMP E	0000	0000
CCCC	CC	OUTPUT	0000	0000
DDDD	DD	OUTPUT	0000	0000
EEEE	EE	XRI **	0000	0000
FFFF	FF	RST 7	0000	0000

Figure 3-7. Mnemonic Mode Display

system under test in a Halt state when the data acquisition cycle is completed. In TRACE SINGLE STEP, the 1611A Halts the μ P system under test after each instruction cycle. The SINGLE STEP mode is functional only in TRACE measurements. During each TRACE execution only one μ P instruction cycle is processed and displayed.

3-21. A TRACE measurement is initiated each time the TRACE key is pressed. Repeated TRACE runs may be made with continuous-run execution. Continuous execution is initiated by pressing TRACE key approximately two seconds. The message CONTINUOUS will be displayed. Pressing the TRACE key again restores regular operation. Continuous runs may be stopped by pressing STOP key or aborted by pressing any other key.

Table 3-1. A80 Memory Transactions Displays

OPCODE	The contents of the data bus is an op-code.
WRITE	The contents of the data bus is information being written to memory.
READ	The contents of the data bus in being read from memory.
INPUT	The contents of the data bus was read from an I/O Port.
OUTPUT	The contents of the data bus is data to be written to an I/O Port.

3-22. **TRACE SETUP.** Enter TRIGGER requirements. Any desired combination of Trigger Enable, Trigger Disable, Trigger Occurrence, and Before or After Trigger requirements may be entered. Ranges of address bus values which will be recognized as Triggers may also be entered with ADDRS BUS $\geq$ or $\leq$ keys. Triggering (including Enable and Disable) may be restricted to certain types of μ P under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press TRACE key.

3-23. Display in TRACE.

3-24. Before the first trigger is detected, two messages may be displayed: (1) WAITING FOR ENABLE flashes until the Enable specification (if entered) is detected; (2) WAITING FOR TRIGGER flashes until the Trigger specification is detected (after the Enable, if specified, has been detected).

3-25. WAITING FOR ENABLE and WAITING FOR TRIGGER can be alternating. This happens when both Enable and Disable are specified and no trigger is found in the window. The Enable is found, no trigger is found, the Disable is found, and the 1611A looks for another Enable.

3-26. After the first Trigger is detected, but before the TRACE measurement is complete, two messages may be displayed: (1) TRIGR OCCUR = shows how many

Triggers are detected from the first Trigger until the Trigger Occurrence specification is met; (2) DELAYING is shown from the time Trigger Occurrence specification is met until the measurement is complete.

3-27. Any data shown below the dashed line will not change until the measurement is complete or until data acquisition is stopped by the STOP key. When a measurement is completed, the Trigger word is shown in an inverse video field, if no AFTER TRIGGER DELAY is specified (figure 3-8). The message LINE 0 also appears. The DISPLAY ROLL keys may be used to move the 16-line display window through the 64 lines (0 to 63) stored in high-speed memory. The LINE message will vary from 0 up to 48. The LINE number shown is the number of the top line in the 16-line display ($48 + 15 = 63$).

ADDRESS		DATA	EXTERNAL	
TRIGGER		8001		
TRIGR OCCUR=10		PRE-TRIGR=5	LINE 0	
ADDRS	OPCODE/DATA		EXTERNAL	
8301	CC	READ	0000	0000
8302	03	READ	0000	0000
830C	3A	OPCODE	0000	0000
8300	01	READ	0000	0000
830E	80	READ	0000	0000
8001	00	READ	0000	0000
830F	1F	OPCODE	0000	0000
8308	02	OPCODE	0000	0000
8301	CC	READ	0000	0000
8302	03	READ	0000	0000
830C	3A	OPCODE	0000	0000
8300	01	READ	0000	0000
830E	80	READ	0000	0000
8001	00	READ	0000	0000
830F	1F	OPCODE	0000	0000
8308	02	OPCODE	0000	0000

Figure 3-8. Trace Display

3-28. IF an incomplete TRACE measurement is stopped by the STOP key, then all data acquired by the high-speed memory during measurement will be displayed (memory dump). If the memory has no new data, then the data display section will be blank. The message STOPPED is shown.

3-29. When a TRACE measurement is incomplete and any key other than an EXECUTE key is pressed, the measurement run is aborted. The display remains as it was before the measurement. Any attempt to change the display with DISPLAY group keys will result in the message RUN ABORTED, NO DISPLAY CHANGE.

3-30. Partial displays (less than 64 memory transactions stored for display) can occur in Trace mode when using a BEFORE TRIGGER specification. The minimum number of lines that will be displayed in ABSOLUTE mode is 64 minus the BEFORE TRIG specification. Internally, the 1611A completes a measurement by counting the number of memory transactions after the Trigger. Because of this, the 1611A may not display the number of memory transaction BEFORE TRIG that have been specified. If a BEFORE TRIG entry of 60 is made, then the 1611A will terminate the measurement 3 memory transactions after the Trigger. This allows for up to 60

memory transactions before the Trigger, the Trigger, and 3 memory transactions after the Trigger to be captured in high-speed memory. If, after the Trace measurement was started, the system under test executed only 15 memory transactions before the Trigger occurred, then the 1611A would display only 19 memory transactions. The ROLL keys can be used to view the 15 transactions before the Trigger, the Trigger, and 3 transactions after the Trigger. The display will not roll up any further once the last memory transaction captured by the 1611A is in the bottom line of the display.

3-31. TRACE TRIGGERS MEASUREMENT EXECUTION.

3-32. TRACE TRIGGERS. In this mode the 1611A captures and displays only memory transactions that match the Trigger specification. For example, the operator may want to see only "Write" operations from a block of memory to verify that proper data was entered. This is easily done by using the Write TRIGGER QUALIFIER switch on Personality Panel A11. The run automatically terminates when 64 Triggers have been found. The run can be terminated before 64 Triggers have been found by using the STOP key.

3-33. TRACE TRIGGERS End on DISABLE. In this mode the TRACE TRIGGERS measurement ends only when Trigger Disable is detected. The 1611A will display up to 64 Triggers that occurred immediately prior to detection of the Disable.

NOTE

Models 1611A with Serial Prefix 1723A and above (Opt A80 installed) have this capability. If Trace Triggers end on Disable mode is desired in Models 1611A with Serial Prefix below 1723A, the old A8 board (01611-66508) must be changed to a modified A8 board (01611-66535).

To enter this mode: (1) Specify a BEFORE TRIG (PRE-TRIGR) of 63; (2) Specify a TRIGGER DISABLE; (3) Press TRACE TRIGS.

3-34. Trace Triggers and Trace Triggers End on Disable displays may be viewed in ABSOLUTE or MNEMONIC mode. In both modes the program or memory address of the Trigger is displayed in the ADRS column. In ABSOLUTE, the machine language op-code or data and the type of μ P machine cycle (e.g., READ, OPCODE, WRITE) are displayed in the OPCODE/DATA column. In MNEMONIC, the assembly language mnemonic and 8 or 16 bit operand (if the operand exists) are displayed in the OPCODE/DATA column. If the operand is not captured by high-speed memory, then *** is shown in the appropriate line of OPCODE/DATA column. Hexadecimal or octal format can be selected and interchanged in both display modes.

3-35. Trace Triggers or Trace Triggers End on Disable measurements can be made in NORMAL or TRACE

THEN HALT modes (selected by TEST MODE switch on Personality Panel A11). In NORMAL, the 1611A captures and displays Triggers while the μ P system under test operates without interruption of program flow. In TRACE THEN HALT, the 1611A places the μ P system under test in a Halt state when the data acquisition cycle is completed.

3-36. A TRACE TRIGGERS or TRACE TRIGGERS End on DISABLE measurement run is initiated each time TRACE TRIGS key is pressed. Repeated runs may be made with Continuous-run execution. Continuous execution is initiated by pressing TRACE TRIGS key approximately two seconds. The message CONTINUOUS will be displayed. Pressing the TRACE TRIGS key again restores regular operation. Continuous runs may be stopped by pressing STOP key or aborted by pressing any other key.

3-37. TRACE TRIGGERS SET-UP. Enter TRIGGER requirements. Trigger Enable and/or Disable requirements may be entered if desired. Ranges of address bus values which will be recognized as Triggers may also be entered with ADDRS BUS $\geq$ or $\leq$ keys. Triggering (including Enable and Disable) may be restricted to certain types of μ P under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press TRACE TRIGS key.

3-38. Display in TRACE TRIGGERS.

3-39. Before the first Trigger is detected two messages may be displayed. (1) WAITING FOR ENABLE flashes until the Enable specification (if entered) is detected. (2) WAITING FOR TRIGGER flashes until the Trigger specification is detected (after the Enable, if specified, has been detected).

3-40. WAITING FOR ENABLE and WAITING FOR TRIGGER can be alternating. This happens when both Enable and Disable are specified and no Trigger is found in the window. The Enable is found, no Trigger is found, the Disable is found, and the 1611A looks for another Enable.

3-41. During TRACE TRIGGERS End on DISABLE measurements, the message TRIGR OCCUR = 0 flashes (instead of WAITING FOR TRIGGER) until the first Trigger is detected.

3-42. After the first Trigger is detected, but before the TRACE TRIGGERS measurement is complete, the message TRIGR OCCUR = may appear. This shows how many Triggers are detected from the first Trigger until high-speed memory is full (64 Triggers Stored).

3-43. In Trace Triggers End on Disable measurements, the message TRIGR OCCUR = >64 can appear for two reasons: (1) When 64 Triggers are detected before the Disable is detected; (2) The 1611A does not contain the TRACE TRIGGERS End on DISABLE modification (1611A with Serial Numbers Prefix below 1723A).

3-44. Any data shown below the dashed line will not change until the measurement is complete or until data acquisition is stopped by the STOP key. When a measurement is completed, the message TRACE TRIGGERS appears. Triggers are shown in the data display (figure 3-9). The message LINE 0 also appears. The DISPLAY ROLL keys may be used to move the 16-line display window through the 64 lines (0 to 63) stored in high-speed memory. The line message will vary from 0 to 48. The LINE number shown is the number of the top line in the 16-line display ($48 + 15 = 63$). TRACE TRIGGERS End on DISABLE measurements can result in partial displays. This is because less than 16 Triggers were detected before Disable.

ADDRESS		DATA	EXTERNAL
TRIGGER		08FX	
TRACE	TRIGGERS	LINE	0
ADDR	OPCODE/DATA	EXTERNAL	
08FE	01 WRITE	0000	0000
08FD	57 WRITE	0000	0000
08FC	00 WRITE	0000	0000
08FB	56 WRITE	0000	0000
08FA	00 WRITE	0000	0000
08F9	56 WRITE	0000	0000
08F8	00 WRITE	0000	0000
08F7	E5 WRITE	0000	0000
08F6	00 WRITE	0000	0000
08F5	56 WRITE	0000	0000
08F4	01 WRITE	0000	0000
08F3	00 WRITE	0000	0000
08F2	16 WRITE	0000	0000
08F1	56 WRITE	0000	0000

Figure 3-9. Trace Triggers Display

3-45. If an incomplete TRACE TRIGGERS or TRACE TRIGGERS End on DISABLE measurement is stopped by the STOP key, then all data acquired by the high-speed memory during the measurement will be displayed (memory dump). If the memory has no new data, then the data display section will be blank. The message STOPPED is shown.

3-46. When a TRACE TRIGGERS or TRACE TRIGGERS End on DISABLE measurement is incomplete and any key other than an EXECUTE key is pressed, the measurement is aborted. The display remains as it was before the measurement. Any attempt to change the display with DISPLAY Group Keys will result in the message RUN ABORTED, NO DISPLAY CHANGE.

3-47. COUNT TRIGGERS MEASUREMENT EXECUTION.

3-48. **COUNT TRIGGERS.** In this mode the 1611A counts Triggers detected between (and including) the Trigger Enable and Trigger Disable words. Count Triggers measurements can be performed in two ways: (1) A regular measurement run is executed each time COUNT TRIGS key is pressed; (2) Repeated COUNT TRIGGERS runs are made with Continuous-run execution. COUNT TRIGGERS measurements are made with TEST MODE

switch on Personality Panel A11 in the NORMAL position.

3-49. A COUNT TRIGGERS measurement run is initiated each time COUNT TRIGS key is pressed. Repeated COUNT TRIGGERS runs may be made with Continuous-run execution (initiated by pressing COUNT TRIGS key approximately two seconds). The message CONTINUOUS will be displayed. Pressing COUNT TRIGS keys again restores regular operation. Continuous runs may be stopped by pressing STOP key or aborted by pressing any other key.

3-50. **COUNT TRIGGERS SET-UP.** Enter Trigger ENABLE, TRIGGER, and Trigger DISABLE requirements. Ranges of address bus values which will be recognized as triggers may also be entered with ADDR BUS $\geq$ or $\leq$ keys. Triggering (including Enable and Disable) may be restricted to certain types of μ P under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press COUNT TRIGS Key.

3-51. Display in COUNT TRIGGERS.

3-52. Before Enable is detected, the message WAITING FOR ENABLE flashes. The bottom line of the data display will show COUNT = 0 TRIGGERS. This line shows the incomplete result of a count in progress. After the Enable is detected, but before the DISABLE is detected, the message COUNTING may flash and the bottom line COUNT = shows how many triggers have been detected. If the cumulative count exceeds $2^{24} - 1$ (approximately 16.78×10^6) Triggers, then the message COUNTER OVERFLOW flashes. This means that the Disable was not detected before the counter limit was exceeded.

3-53. When the Disable is detected the measurement is completed (figure 3-10). The bottom line of the data display COUNT = disappears. The top line of the data display COUNT = shows how many Triggers were detected between (and including) the Enable and Disable. MAX = and MIN = show the same number of Triggers detected as COUNT=. This is because both the maximum and minimum results of the first COUNT TRIGS run are the same as the completed measurement result.

3-54. In COUNT TRIGGERS Continuous-run execution, the bottom line COUNT = will often be flashing. This is due to updating of the incomplete result of a count in progress. The top line COUNT = shows the result of the last measurement completed. MAX = shows the maximum number of Triggers detected by any of the repeated executions of Count Triggers. MIN = shows the minimum number of Triggers detected by any of the repeated executions of Count Triggers.

3-55. Any COUNT TRIGGERS measurement in progress may be stopped with the STOP key or aborted with any other key. When the STOP key is pressed while a run is in progress, the message STOPPED appears.

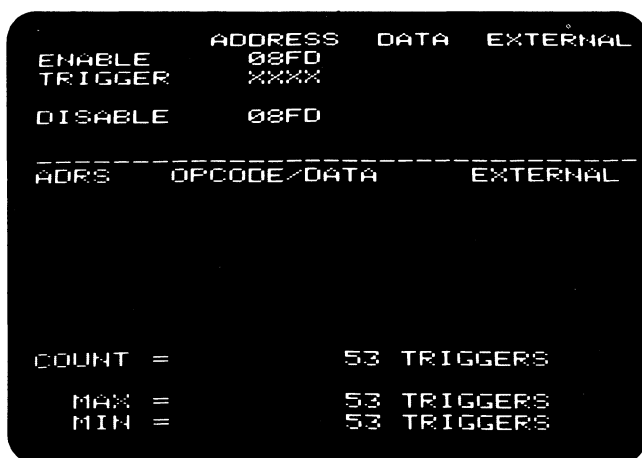


Figure 3-10. Count Triggers Display

3-56. TIME INTERVAL MEASUREMENT EXECUTION.

3-57. TIME INTERVAL. This mode produces a readout of elapsed time between the occurrence of two states defined by Trigger Enable and Trigger Disable. The timing measurement is made using an internal 1 MHz reference oscillator. Accuracy is within $0.1\% \pm 1\mu s$. Verifying the execution time of wait loops is one application of the time interval feature. It is also useful for measuring time required for the execution of a subroutine when a critical timing interface is involved with the system hardware or an external device. Time Interval measurements can be performed in two ways: (1) A regular measurement run is executed each time TIME INTVL key is pressed; (2) Repeated TIME INTERVAL runs are made with Continuous-run execution. Time Interval measurements are made with TEST MODE switch on Personality Panel A11 in the NORMAL position.

3-58. A TIME INTERVAL measurement run is initiated each time TIME INTVL key is pressed. Repeated TIME INTERVAL runs may be made with Continuous-run execution. This is initiated by pressing TIME INTVL key approximately two seconds. The message CONTINUOUS will be displayed. Pressing TIME INTVL key again restores regular operation. Continuous runs may be stopped with STOP key or aborted by pressing any other key.

3-59. TIME INTERVAL SET-UP. Enter Trigger ENABLE and Trigger DISABLE requirements. NO TRIGGER entry is required. The Enable and Disable may both be restricted to certain types of μP under test machine cycles with the TRIGGER QUALIFIER switches on Personality Panel A11. Press TIME INTVL key.

3-60. Display in TIME INTERVAL.

3-61. Before the Enable is detected, the message WAITING FOR ENABLE flashes. The bottom line of the data

display will show TIME = 0 MICROSECONDS. This line shows the incomplete result of a count in progress. After the Enable is detected, but before the DISABLE is detected, the message COUNTING may flash and the bottom line TIME = shows the elapsed time in microseconds. If the cumulative count exceeds $2^{24} - 1$ (approximately 16 seconds), then the message COUNTER OVERFLOW flashes. This means that the Disable was not detected before the counter limit was exceeded.

3-62. When the Disable is detected the measurement is completed (figure 3-11). The bottom line of the data display TIME = disappears. The top line of the data display TIME = shows elapsed time in microseconds between occurrence of the Enable and the Disable. MAX = and MIN = will show the same elapsed time as TIME =. This is because both maximum and minimum results of the first TIME INTVL run are the same as the completed measurement result.

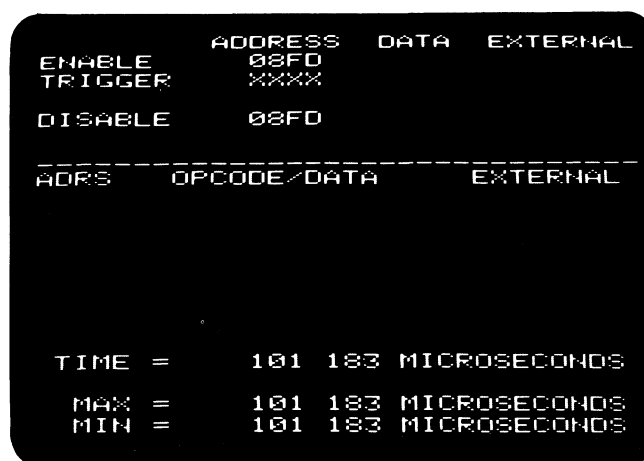


Figure 3-11. Time Interval Display

3-63. In TIME INTERVAL Continuous-run execution, the bottom line TIME = will often be flashing. This is due to updating of the incomplete result of a count in progress. The top line TIME = shows the result of the last measurement completed. MAX = shows maximum elapsed time of any repeated executions of Time Interval. MIN = shows minimum elapsed time of any repeated executions of Time Interval.

3-64. All TRIGGER field entries are ignored by the 1611A in Time Interval mode. Any Time Interval measurement in progress may be stopped with the STOP key or aborted with any other key.

3-65. OPERATOR'S CHECKS.

3-66. SELF-TEST. When power is applied to the 1611A, the internal microprocessor automatically performs an

internal self-test on the 1611A. A check sum is performed to verify contents of the ROM. Next, a test pattern is written to the RAM (to check for RAM ERROR), then read back and checked for accuracy. Also, some system hardware (most of the circuitry on A7 and A8 boards) is tested at this time. Upon completion of these tests, the message SELF-TEST COMPLETED is written on screen by the microprocessor to give a visual indication that the display circuitry and microprocessor are working properly. If a malfunction is detected, then the messages ERROR IN RAM, ERROR IN ROM, or ERROR IN HARDWARE may be displayed. These give quick indications of where to look when 1611A troubleshooting is necessary.

3-67. PROBE TEST. Functional tests may be made on the 1611A without any external circuits by connecting the microprocessor probe plug into the Personality Panel Probe Test socket. Executing a trace generates a test display (see figure 3-12). Most system functions and controls may then be exercised on this pattern. In addition to generating a test pattern, the PROBE TEST feature permits checkout of Personality Panel indicators by cycling through NO CLOCK, HOLD, WAIT, and INTERRUPT ENABLE and HALT lights at a 1-Hz rate. Check WAIT/HOLD BY 1611A light by setting TEST MODE switch to SINGLE STEP. Return TEST MODE switch to NORMAL.

3-68. STATUS MESSAGES. The following messages are displayed on the 1611A screen to provide an indication of 1611A operating status. (Messages may vary with different 1611A options.)

CONTINUOUS: Appears after an EXECUTE key has been held down approximately two seconds, which initiates continuous-run execution. Single run is restored by pressing the same key briefly. Continuous operation is stopped by STOP key, or aborted by pressing any other key.

COUNTER OVERFLOW: Appears in COUNT TRIGS or TIME INTERVAL mode when event counters overflow (Count exceeds $2^{24} - 1$).

COUNTING: Appears in COUNT TRIGS or TIME INTERVAL mode when 1611A is in the process of counting.

DELAYING: Displayed in TRACE mode from the time Trigger Occurrence specification has been met until the measurement is complete.

ERROR IN HARDWARE: Displayed when 1611A self-test has detected a malfunction in its internal hardware (on A7 or A8 boards).

ERROR IN RAM/ROM: Appropriate message appears when self-test display comes on after turn-on if 1611A determines that random-access memory or read only memory is not functioning correctly.

ILLEGAL CHARACTER: Appears if the operator attempts to enter an unacceptable character into an open trace specification field. For example, attempting to enter an alpha character in the BEFORE TRIG field (decimal field) will generate this message.

LINE 0 - 48: Indicates line number of top line in data display in TRACE and TRACE TRIGGERS modes. When LINE 48 is displayed, the next 15 lines on the display complete the 64 lines (0 to 63) stored in memory.

NO OPEN DATA FIELD: Displayed when the operator tries to enter a character from the ENTRY field without pressing appropriate key in the TRACE SPECIFICATION keyboard section to open a data field.

RUN ABORTED, NO DISPLAY CHANGE: Displayed for two conditions:



Figure 3-12. Probe Test Display

1. If a DISPLAY key is pressed when a TRACE or TRACE TRIGS run is in progress (WAITING FOR ENABLE, WAITING FOR TRIGGER, or the required number of TRIGR OCCUR has not been met).
2. If a DISPLAY key is pressed after a previous TRACE or TRACE TRIGS measurement run has been aborted by pressing any key other than an EXECUTE key while run is in progress.

SELF-TEST COMPLETED: Indicates satisfactory completion of self-test (unless an error message is also displayed).

SINGLE STEP: Displayed after TRACE is pressed in single-step mode.

SINGLE STEP, NO DISPLAY CHANGE: Displayed when an attempt is made to change the display by using DISPLAY keys after a trace has been executed in TRACE SINGLE STEP test mode.

SINGLE STEP, TRACE ONLY: Displayed when TEST MODE switch is set to SINGLE STEP and TRACE TRIGS, COUNT TRIGS, or TIME INTVL in the keyboard EXECUTE field is pressed. Only TRACE can be executed in SINGLE STEP test mode.

STOPPED: Displayed when STOP key is pressed, indicates a halt of any EXECUTE run in progress.

TRIGR OCCUR =: Displayed for three conditions:

1. During TRACE measurements, from first trigger recognition until number of triggers recognized equals the number selected by trigger occurrence specification.

2. During TRACE TRIGS measurements, from first trigger recognition until display memory is full (64 triggers stored).
3. During TRACE TRIGS End on Disable measurements, TRIGR OCCUR = 0 is displayed until first trigger is found, and TRIGR OCCUR = >64 is displayed if 64 triggers have been found without finding the Disable word, or if the 1611A does not contain the Trace Triggers End on Disable hardware modification (1611A with Serial Number Prefix below 1723A).

NOTE

If Trace Triggers End on Disable mode is desired, the old A8 board (01611-66508) may be changed to A8 board (01611-66535).

WAITING FORENABLE: Only displayed when a Trigger Enable has been specified and one of three conditions exists:

1. ENABLE specification has not been met.
2. System under test is running poorly or not at all.
3. This message will alternate with WAITING FOR TRIGGER if a trigger is not found between trigger ENABLE and DISABLE specifications, but the DISABLE is being found so the search for ENABLE is resumed.

WAITING FOR TRIGGER: Displayed for two conditions:

1. During TRACE and TRACE TRIGS measurements after Trigger ENABLE specification has been met, if an ENABLE has been specified, but before the first trigger has been detected.
2. Enable has not been specified and system under test is running poorly or not at all.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section provides two types of performance tests: an Operation Verification and a Specification Verification. The Operation Verification provides approximately 90% assurance that the 1611A Option A80 is functioning properly. The Specification Verification checks electrical parameters of the instrument using the specifications in table 1 as the performance standards. Unless the detailed specification Verification is required, it is recommended that only the Operation

Verification be performed. All tests can be performed without access to the interior of the instrument.

4-3. PERFORMANCE TEST RECORD.

4-4. Performance Test results may be recorded in the Performance Test Record at the end of the procedures. The test record lists all tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

4-5. OPERATION VERIFICATION.

4-6. To assure that the 1611A Option A80 is operating properly without testing all the specifications listed in table 1, perform the following Operating Verification.

4-7. SELF-TEST

DESCRIPTION:

This test verifies proper operation of the ROM, display RAM, and some hardware circuits. If the ROM/RAM hardware test fails, the test will be repeated and a display indicating the failed circuit will be generated. When self test passes, a display is generated to indicate the circuit is operating properly.

PROCEDURE:

- a. Set power LINE switch to on. Verify that CRT displays message SELF TEST COMPLETED.

PERFORMANCE TESTS

4-8. MEMORY DISPLAY TEST.

DESCRIPTION:
This test verifies that the 1611A storage memory can be loaded and the information stored in memory can be viewed through a 16 line movable window. This test also verifies that information is being sensed correctly by the address and data lines.

- PROCEDURE:**
- a. Connect μ P probe A13 to front panel PROBE TEST socket.
 - b. Set 1611A front panel controls as follows:

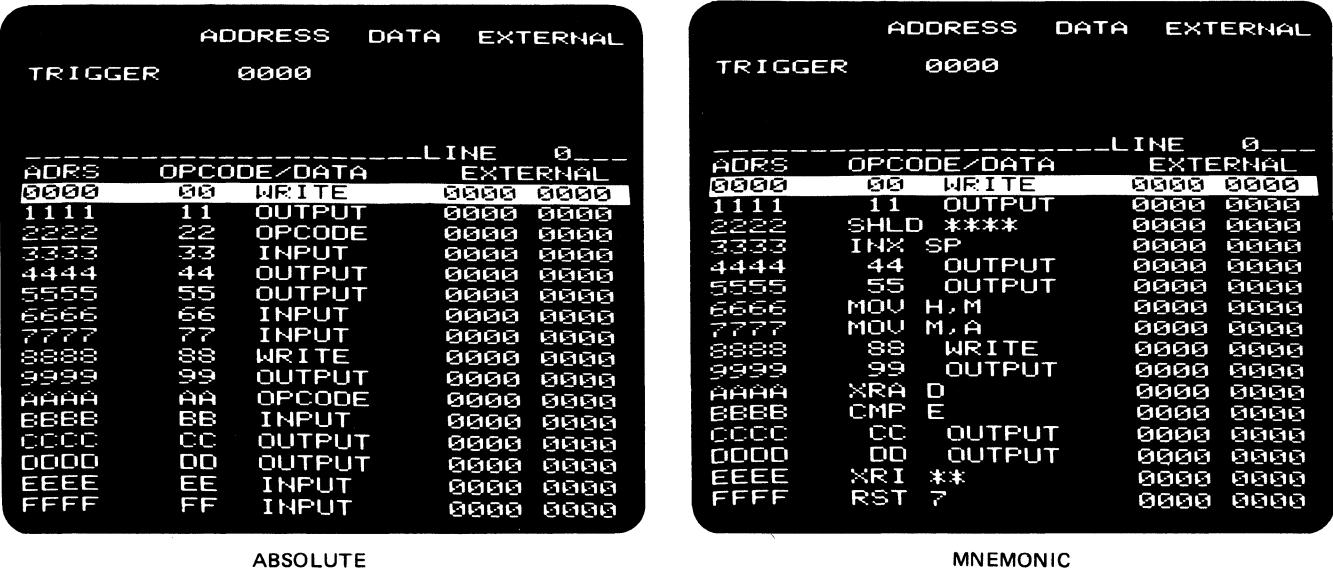
ADRS·DATA BUS	HEXADECIMAL
I/O	OFF
WRITE	OFF
READ OP CODE	OFF
READ OP CODE	OFF
TEST MODE	NORMAL

- c. Press TRACE key. Verify that a list is displayed.
- d. Use ROLL keys to scroll through memory. Verify that LINE 0 through LINE 48 can be displayed.

NOTE

It may be necessary to use ABSOLUTE/MNEMONIC key to view all 64 lines of memory.

- e. Press TRIGGER/ADDRESS BUS = key.
- f. Enter 0000.
- g. Press TRACE key. Verify the following display is shown in ABSOLUTE or MNEMONIC modes as below:



PERFORMANCE TESTS

4-9. STATUS MESSAGES FOR TRACE MODE TEST.**DESCRIPTION:**

This test verifies that two messages are displayed before the first trigger condition is detected. WAITING FOR ENABLE flashes until the Enable specification (if entered) is detected. WAITING FOR TRIGGER flashes until the Trigger specification is detected.

PROCEDURE:

- a. Press TRIGGER ENABLE/ADDRESS BUS = key.
 - b. Enter CDEF.
 - c. Press TRACE. Verify that WAITING FOR ENABLE message is flashing.
 - d. Press TRIGGER ENABLE/ADDRESS BUS = key.
 - e. Press DON'T CARE.
 - f. Press TRIGGER/ADDRESS BUS = key.
 - g. Enter 89AB.
 - h. Press TRACE key. Verify that WAITING FOR TRIGGER message is flashing.
-

4-10. TRIGGER $\leq$, $\geq$, TRIGGER OCCURRENCES, DELAY AND TRACE TRIGGERS TEST.**DESCRIPTION:**

This test verifies that the 1611A can recognize $\leq$ or $\geq$ trigger specification, count trigger occurrences, and count delay before the memory is loaded and a display is generated. This test also verifies that in TRACE TRIGGERS, only information matching Trigger conditions is stored in memory and displayed.

PROCEDURE:

- a. Press ADRS BUS $\geq$ key.
- b. Enter 0000.
- c. Press ADRS BUS $\leq$ key.
- d. Enter 1110.
- e. Press TRIGGER OCCURRENCE key.
- f. Enter 256.
- g. Press AFTER TRIG key.
- h. Enter 65472.
- i. Press TRACE key. WAITING FOR TRIGGER message may flash briefly. Verify that DELAYING message flashes until trace is completed (LINE 0 displayed.)
- j. Press TRACE TRIGGERS. Verify that every row of data display shows:

ADRS
0000

OPCODE/DATA
00 WRITE

EXTERNAL
0000 0000

It may be necessary to use ABSOLUTE/MNEMONIC key to obtain this display.

PERFORMANCE TESTS

4-11. TRACE TRIGGERS END ON DISABLE TEST.**DESCRIPTION:**

This test verifies that the 1611A can execute a TRACE TRIGGERS function which terminates only when a Triggers Disable condition is detected.

PROCEDURE:

- a. Press and hold DON'T CARE key approximately three seconds until all TRACE SPECIFICATIONS are cleared.
- b. Press TRIGGER/ADDRESS BUS = key.
- c. Enter 0000.
- d. Press BEFORE TRIG key.
- e. Enter 63.
- f. Press TRIGGER DISABLE/ADDRESS BUS = key.
- g. Enter ABAB.
- h. Press TRACE TRIGS.
- i. Verify that TRIG OCCUR = > 64 message flashes.
- j. Press TRIGGER DISABLE/ADDRESS BUS = key.
- k. Enter FFFF.
- l. Press TRACE TRIGS key.
- m. Verify that data display shows only one line as follows:

ADRS
0000

OPCODE/DATA
00 WRITE

EXTERNAL
0000 0000

It may be necessary to use the ABSOLUTE/MNEMONIC key to obtain this result.

NOTE

If your 1611A serial number prefix is below 1723A, then TRIG OCCUR = > 64 is displayed immediately to indicate that the 1611A does not have Trace Triggers End On Disable capability.

4-12. PRETRIGGER TEST.**DESCRIPTION:**

This test verifies the ability to view a specified number of memory transactions that occur before a selected trigger word.

PROCEDURE:

- a. Clear all TRACE SPECIFICATIONS entered on display by pressing the DON'T CARE key for approximately three seconds until all TRACE SPECIFICATIONS are cleared.
 - b. Press TRIGGER/ADDRESS BUS = key.
 - c. Enter AAAA.
 - d. Press BEFORE TRIGGER key.
 - e. Enter 4.
 - f. Press TRACE key. Verify that trigger word AAAA, in inverse video, is located on the 5th line of the display.
-

PERFORMANCE TESTS

4-13. COUNT TRIGGER TEST AND STOP TEST.**DESCRIPTION:**

This test verifies that the 1611A can count Triggers detected between (and including) the Trigger Enable and Trigger Disable words. The test also verifies that operation is halted and STOPPED message is displayed when STOP key is pressed.

PROCEDURE:

- a. Clear all TRACE SPECIFICATIONS entered on display by pressing the appropriate field selection keys and then pressing DON'T CARE key.
 - b. Press TRIGGER ENABLE/ADDRESS BUS = key.
 - c. Enter 0000.
 - d. Press TRIGGER DISABLE/ADDRESS BUS = key.
 - e. Enter FFFF.
 - f. Press TRIGGER/ADDRESS BUS = key.
 - g. Enter 4444.
 - h. Press and hold COUNT TRIGS key for approximately three seconds until CONTINUOUS message is displayed. Verify that COUNT =, MAX =, and MIN =, all display 1 TRIGGERS.
 - i. Press STOP key and verify that STOPPED message is displayed.
-

4-14. TIME INTERVAL TEST.**DESCRIPTION:**

This test verifies that the 1611A can count the time interval occurring between states determined by Trigger Enable and Trigger Disable specifications. If no Trigger Disable condition is found, the COUNTER OVERFLOW, message occurs after approximately 16 seconds.

PROCEDURE:

- a. Clear all TRACE SPECIFICATIONS entries on the display by pressing and holding the DON'T CARE key approximately three seconds until all TRACE SPECIFICATIONS are cleared. (NO OPEN DATA FIELD message will flash until the clear is complete.)
 - b. Press TRIGGER ENABLE/DATA BUS = key.
 - c. Enter 00.
 - d. Press TRIGGER DISABLE/DATA BUS = key.
 - e. Enter FF.
 - f. Press and hold TIME INTVL key for approximately three seconds until CONTINUOUS message is displayed. Verify that TIME =, MAX =, and MIN =, all display 120 microseconds (± 1).
 - g. Press TRIGGER DISABLE/DATA BUS = key.
 - h. Enter AB.
 - i. Press TIME INTVL key. Verify that COUNTING, followed by COUNTER OVERFLOW messages are displayed (flashing).
-

PERFORMANCE TESTS

4-15. TRIGGER QUALIFIER SWITCH TEST.**DESCRIPTION:**

This test verifies that the TRIGGER QUALIFIER switches can restrict triggering of the 1611A to certain types of machine cycles.

PROCEDURE:

- a. Clear TRACE SPECIFICATIONS on the display by pressing and holding the DON'T CARE key for approximately three seconds until all TRACE SPECIFICATIONS are cleared.
- b. Press TRACE key. Verify that list is displayed.
- c. Set OCTAL/HEXADECIMAL switch to each position and verify that displayed data converts to selected base.
- d. Set TRIGGER QUALIFIER I/O switch to I/O position.
- e. Press TRACE key. Verify that inverse video trigger displays INPUT or OUTPUT in the OPCODE/DATA column. It may be necessary to use ABSOLUTE/MNEMONIC key to obtain this display.
- f. Return I/O switch to OFF.
- g. Set WRITE switch to WRITE position.
- h. Press TRACE key. Verify that inverse video trigger displays WRITE in the OPCODE/DATA column.
- i. Return WRITE switch to OFF position.
- j. Set READ $\overline{\text{OP CODE}}$ switch to $\overline{\text{OP CODE}}$ position.
- k. Press TRACE key. Verify that WAITING FOR TRIGGER message is flashing.
- l. Return $\overline{\text{OP CODE}}$ switch to OFF.
- m. Set READ OP CODE switch to OP CODE position.
- n. Press TRACE key. Verify that inverse video trigger displays OPCODE read or write in the OPCODE/DATA column. It may be necessary to use ABSOLUTE/MNEMONIC key to obtain this display.
- o. Return OP CODE switch to OFF.
- p. Verify that NO CLOCK, HOLD, WAIT, INTERRUPT ENABLE, and HALT indicators light in sequence.
- q. Set TEST MODE switch to TRACE SINGLE STEP. Verify that WAIT/HOLD by 1611A indicator is on.
- r. Return TEST MODE switch to NORMAL.
- s. Check TRIGGER QUALIFIER indicator by cycling I/O, WRITE, $\overline{\text{OP CODE}}$, and OP CODE switches on and off. All TRIGGER QUALIFIER switches must be OFF for TRIGGER QUALIFIER indicator to be extinguished.

END OF OPERATION VERIFICATION TESTS.

PERFORMANCE TESTS

4-16. SPECIFICATION VERIFICATION.

4-17. The following procedures test the electrical parameters of the 1611A Option A80 using the specifications of table 1-1 as the performance standard. Threshold specifications are tested by applying the minimum voltage that the 1611A will recognize as logic "1" and the maximum voltage that the 1611A will recognize as a logic "0". Setup time is the minimum time that data must be present at a 1611A probe input before it can be clocked into the 1611A. Hold time is the minimum time that data must be present at a 1611A probe input after it is clocked into the 1611A. When the minimum threshold, setup time, and hold time specifications are met, then known data that is clocked into the 1611A can be shown by the CRT (or front-panel indicators) to verify proper 1611A circuit operation.

4-18. TEST SIGNAL CONNECTIONS. No standard adapter is available for connecting test signals to microprocessor probe A13. Therefore, it is recommended that short lengths of small-gauge solid wire be inserted in the probe socket and that test signals be connected to these wires with a BNC-to-alligator clip adapter. The solid wires allow socket clamping action to secure a good connection between the signal source and the probe.

NOTE

Some tests will not give correct results if the wrong 1611A keys are accidentally pressed. If the 1611A does not give a correct indication, cycle LINE power switch off and on, and then repeat the test to verify that the incorrect indication was not caused by pressing the wrong key.

4-19. INITIAL SETUP.

- a. Connect external probe A12 and μ P probe A13 to their respective connectors on 1611A rear panel. Do not connect μ P probe A13 to front-panel test socket.
- b. Set 1611A front-panel controls as follows:

ADRS·DATA BUS	HEXADECIMAL
READ OP CODE	OFF
READ OP CODE	OFF
WRITE	OFF
I/O	OFF
TEST MODE	NORMAL

NOTE

Perform tests in the sequence given. Test equipment should not be disconnected unless specified in the procedure. Remove μ P probe cable with 40-pin male connector from μ P probe A13 during these tests. Do not specify an ENABLE. Specify TRIGGER = DON'T CARE.

PERFORMANCE TESTS**4-20. CLOCK TEST.****SPECIFICATION:**

Repetition rate: 300 kHz to 4 MHz.

Threshold: Logic 1 (HI) +9 V to +13 V;

Logic 0 (LO) -1.0 V to +0.8 V.

DESCRIPTION:

A logic pulse that satisfies minimum pulse width and maximum frequency is applied to the 1611A μ P probe A13 CLOCK input. The front panel NO CLOCK indicator light is then checked to verify proper operation.

EQUIPMENT:

Pulse generator (1) HP 8013B

BNC-to-Alligator Clip Adapter (1) HP P/N 8120-1292

Oscilloscope (1) HP 1740A

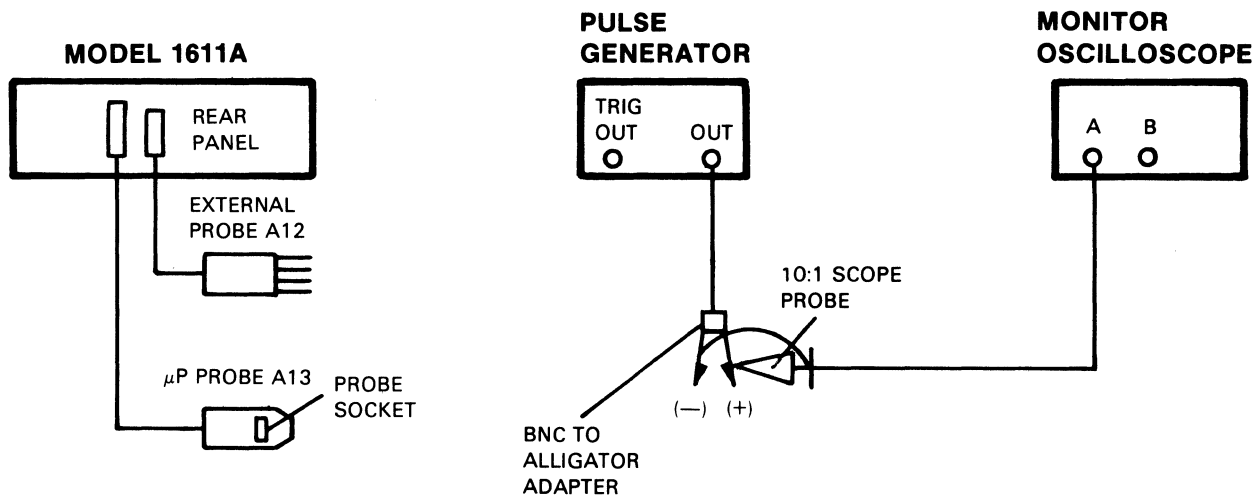


Figure 4-2. Clock Line Test Setup

PROCEDURE:

- a. Connect test equipment as shown in figure 4-2.
- b. Verify that NO CLOCK indicator light is on.
- c. Connect pulse generator output between pin 15 (Φ 2) and pin 2 (GND) of μ P probe A13 test socket.
- d. Adjust pulse generator for output shown in figure 4-3A.

PERFORMANCE TESTS

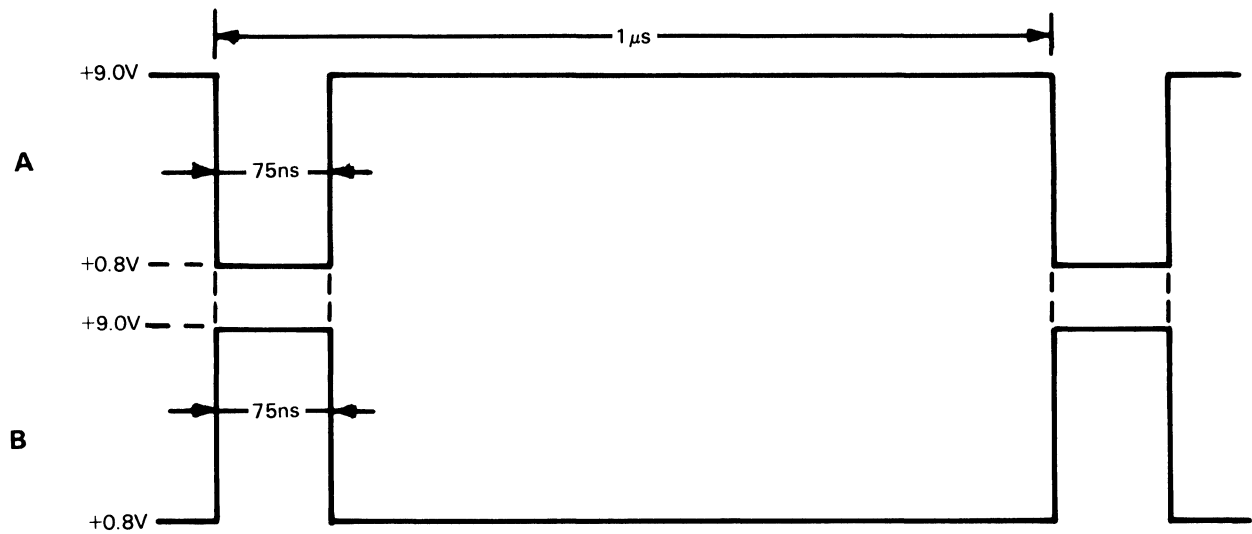


Figure 4-3. Clock Test Waveforms

- e. Verify that NO CLOCK indicator light is off.
- f. Adjust pulse generator output for waveform shown in figure 4-3B.
- g. Verify that NO CLOCK indicator light is off.

PERFORMANCE TESTS

4-21. WAIT, HLDA, and INTE LINES TEST.

SPECIFICATION:

Threshold: Logic 1 (HI) +3 V to +6 V;
Logic 0 (LO) -1.0 V to +0.8 V.

DESCRIPTION:

A high pulse (logic 1) that satisfies minimum threshold is applied to μ P probe A13 WAIT, HLDA, and INTE inputs and clocked into the 1611A. The front panel indicators are then checked to verify proper operation.

EQUIPMENT:

Pulse Generators (2)	HP 8013B
BNC-to-Alligator Clip Adapters (2)	HP P/N 8120-1292
Oscilloscope (1)	HP 1740A

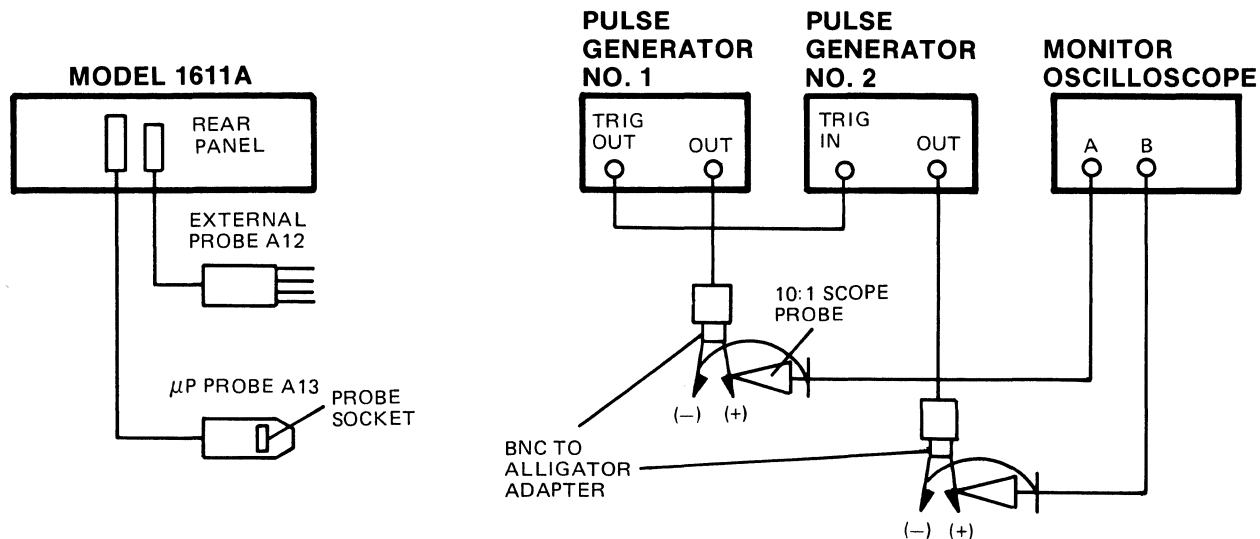


Figure 4-4. Wait, HLDA, and Inte Test Setup

PROCEDURE:

- a. Connect test equipment as shown in figure 4-4.
- b. Connect pulse generator No. 1 between pin 15 (Φ 2) and pin 2 (GND) of microprocessor probe A13 test socket.
- c. Connect pulse generator No. 2 between pin 16 (INTE) and pin 2 (GND) of μ P probe A13.
- d. Adjust pulse generators for waveforms shown in figure 4-5.

PERFORMANCE TESTS

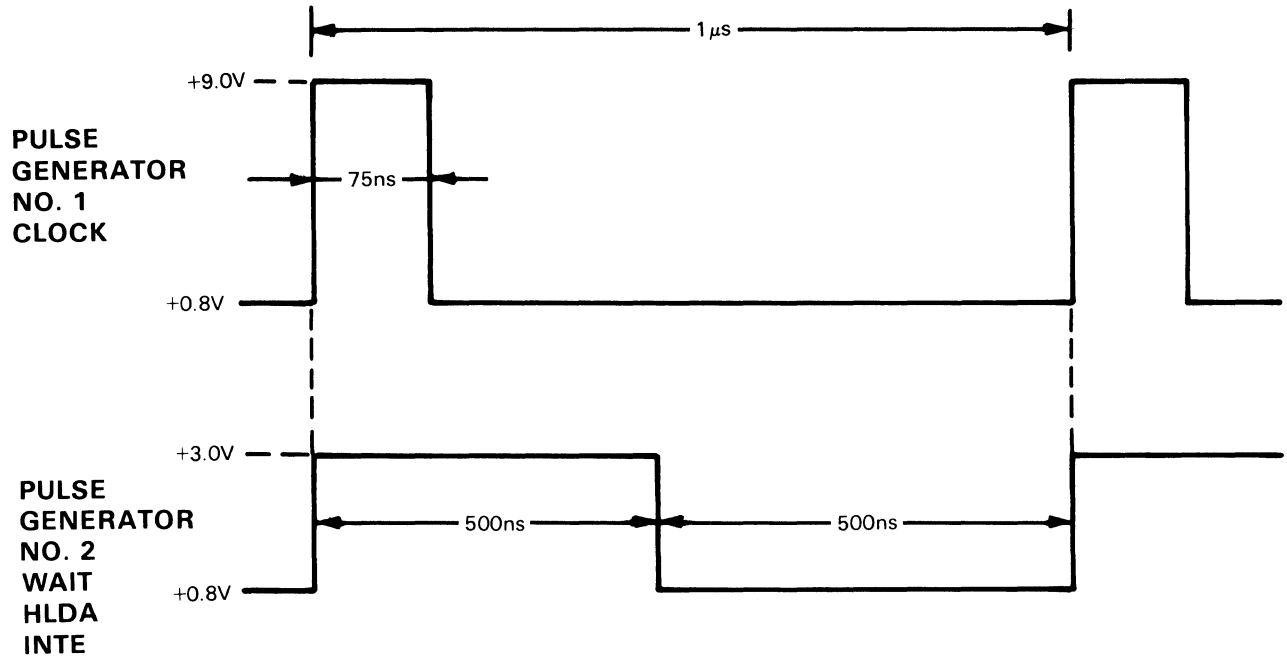


Figure 4-5. Wait, HLDA, and Inte Test Waveforms

- e. Verify that personality panel INTERRUPT ENABLE indicator light is on.
- f. Disconnect pulse generator No. 2 from pin 16 (INTE) of μP probe A13.
- g. Connect pulse generator No. 2 between pin 24 (WAIT) and pin 2 (GND) of μP probe A13 test socket.
- h. Verify that personality panel WAIT indicator light is on.
- i. Disconnect pulse generator No. 2 from pin 24 (WAIT) of μP probe A13.
- j. Connect pulse generator No. 2 between pin 21 (HLDA) and pin 2 (GND) of μP probe A13 test socket.
- k. Verify that personality panel HOLD indicator light is on.

PERFORMANCE TESTS**4-22. READY LINE TEST.****SPECIFICATION:**

Setup time: ≥ 80 ns relative to falling edge of $\Phi 2$.

Hold time: ≥ 0 ns relative to falling edge of $\Phi 2$.

Threshold: Logic 1 (HI) +3 V to +6 V;

Logic 0 (LO) -1.0 V to +0.8 V.

DESCRIPTION:

A high pulse (logic 1) that satisfies minimum setup time, hold time, and threshold is applied to the μ P READY input and clocked into the 1611A. The SYNC input is connected to +5 V to enable the READY input. The CRT display is then checked to verify proper operation.

EQUIPMENT:

Pulse Generator (2)	HP 8013B
BNC-to-Alligator Clip Adapter (3)	HP P/N 8120-1292
Oscilloscope (1)	HP 1740A
Power Supply (1)	HP 6213A

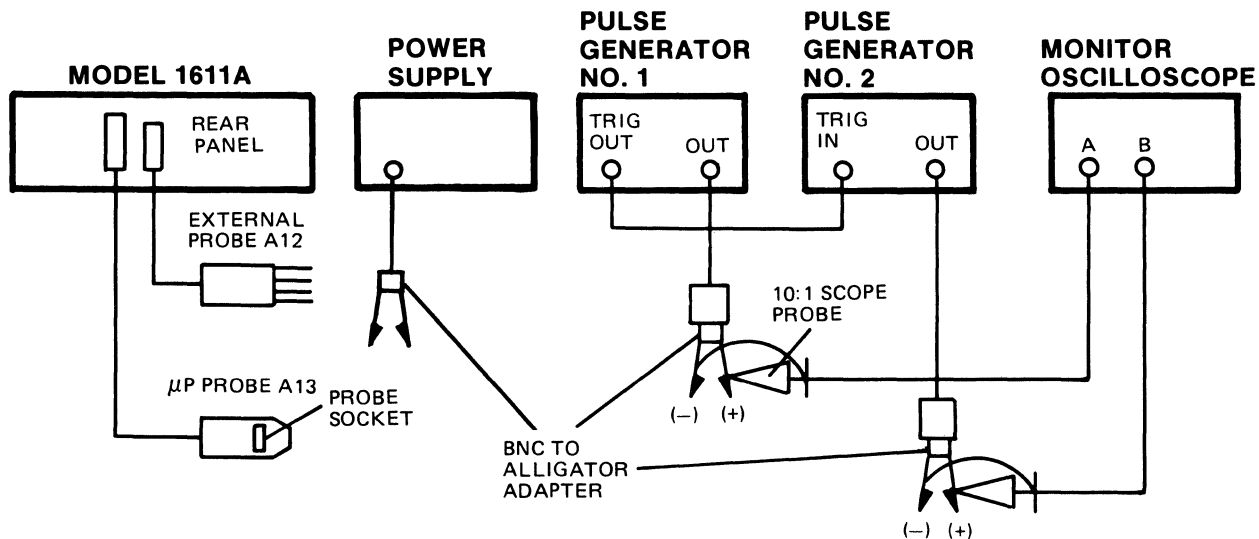


Figure 4-6. Ready Line Test

PROCEDURE:

- Connect test equipment as shown in figure 4-6.
- Connect +5 V from power supply between pin 19 (SYNC) and pin 2 (GND) of μ P probe A13 test socket.
- Connect pulse generator No. 1 between pin 15 ($\Phi 2$) and pin 2 (GND) of μ P probe A13 test socket.

PERFORMANCE TESTS

- d. Connect pulse generator No. 2 between pin 23 (READY) and pin 2 (GND) of μ P probe A13 test socket.
- e. Adjust pulse generators for waveforms shown in figure 4-7.

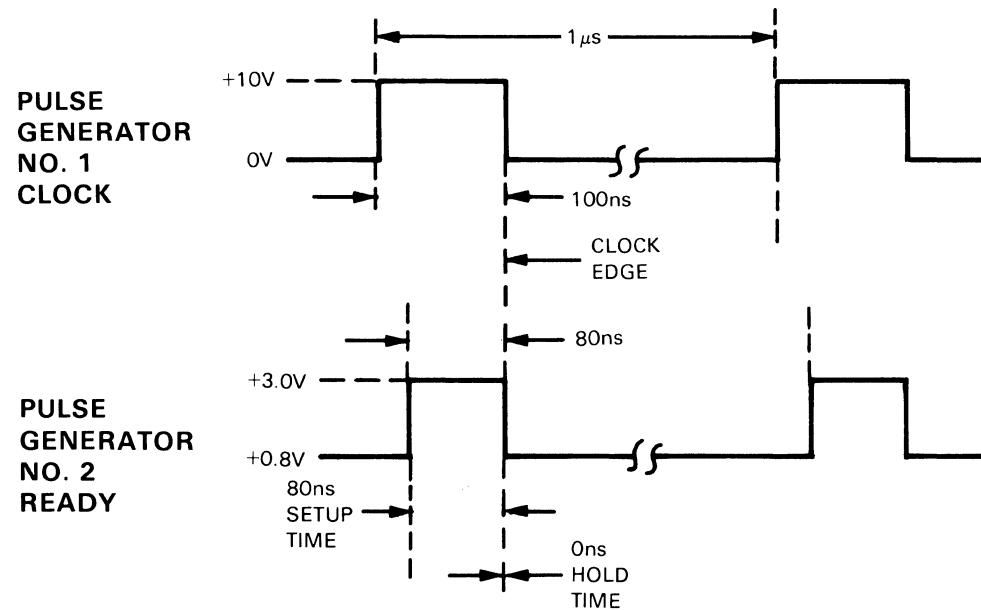


Figure 4-7. Ready Line Test Waveforms

- f. Press TRACE key. Verify that a list is displayed.

PERFORMANCE TESTS

4-23. SYNC LINE TEST.

SPECIFICATION:

Setup time: ≥ 100 ns relative to falling edge of $\Phi 2$.

Hold time: ≥ 25 ns relative to falling edge of $\Phi 2$.

Threshold: Logic 1 (HI) +3 V to +6 V;

Logic 0 (LO) -1.0 V to +0.8 V.

DESCRIPTION:

A high pulse (logic 1) that satisfies minimum threshold, setup time, and hold time is applied to μ P probe A13 SYNC input and clocked into the 1611A. The CRT display is then checked to verify proper operation. The READY input of μ P probe A13 is connected to -5 V to enable the SYNC input.

EQUIPMENT:

Pulse Generator (2)	HP 8013B
BNC-to-Alligator Clip Adapter (3)	HP P/N 8120-1292
Oscilloscope (1)	HP 1740A
Power Supply (1)	HP 6213A

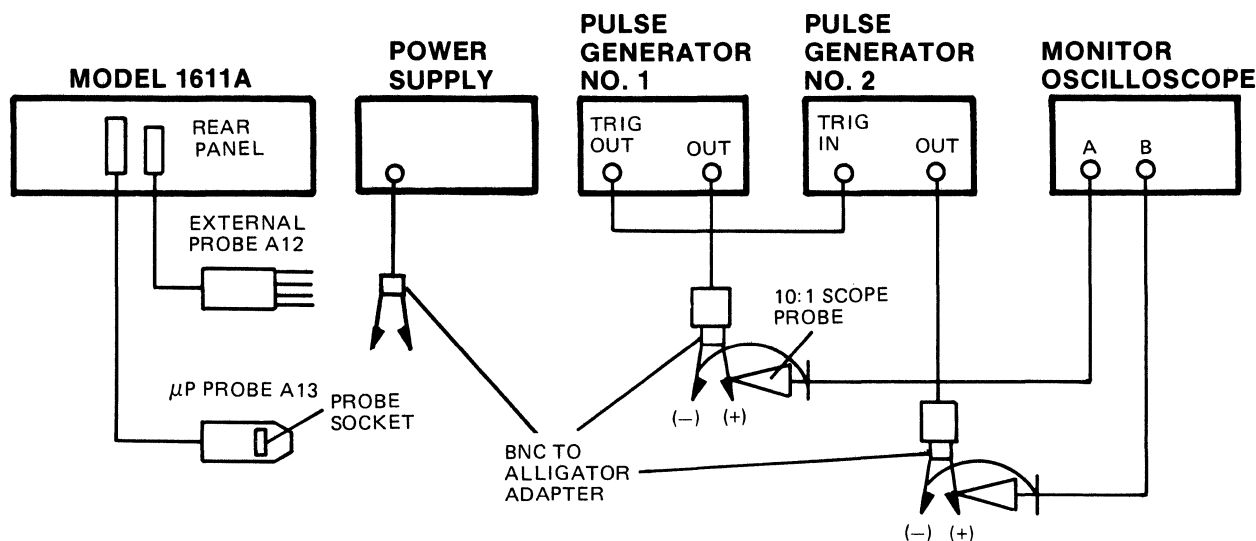


Figure 4-8. Sync Test Setup

PROCEDURE:

- Connect test equipment as shown in figure 4-8.
- Connect +5 V from power supply between pin 23 (READY) and pin 2 (GND) of μ P probe A13 test socket.
- Connect pulse generator No. 1 between pin 15 ($\Phi 2$) and pin 2 (GND) of μ P probe A13 test socket.

PERFORMANCE TESTS

- d. Connect pulse generator No. 2 between pin 19 (READY) and pin 2 (GND) of μ P probe A13 test socket.
- e. Adjust pulse generators for waveforms shown in figure 4-9.

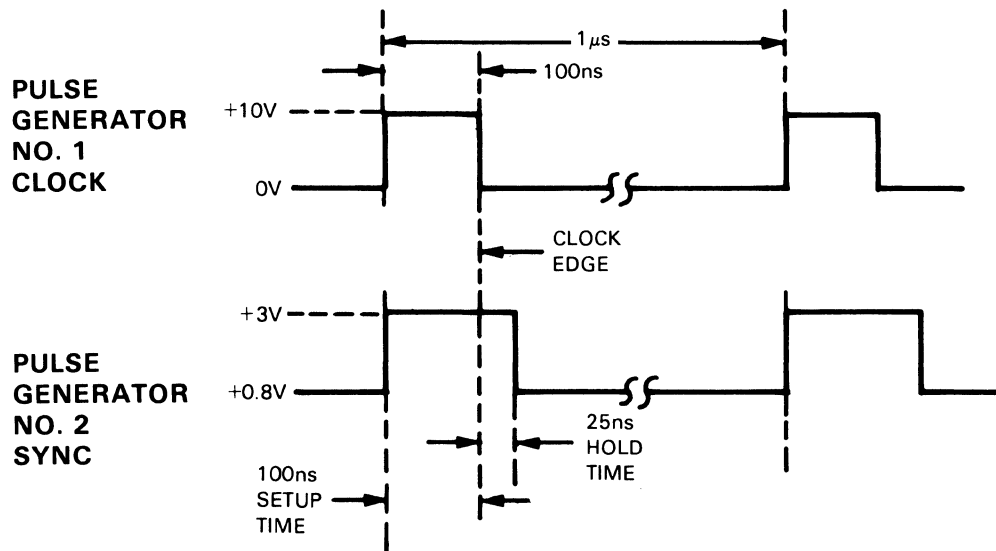


Figure 4-9. Sync Test Waveforms

- f. Press TRACE key. Verify that a list is displayed.

PERFORMANCE TESTS

4-24. ADDRESS LINES TEST.

SPECIFICATION:

Setup time: ≥ 100 ns relative to rising edge of $\Phi 2$.

Hold time: ≥ 25 ns relative to rising edge of $\Phi 2$.

Threshold: Logic 1 (HI) +3 V to +6 V;

Logic 0 (LO) -1.0 V to $+0.8$ V.

DESCRIPTION:

A high pulse (logic 1) that satisfies minimum setup time, hold time, and threshold is applied to each address line input and clocked into the 1611A. The CRT display is then checked to verify proper operation of the line under test. The READY and SYNC inputs of μ P probe A13 is connected to +5 V to enable data to be clocked into the 1611A.

EQUIPMENT:

Pulse Generator (2)	HP 8012B
BNC-to-Alligator Clip Adapter (3)	HP P/N 8120-1292
Oscilloscope (1)	HP 1740A
Power Supply (1)	HP 6213A

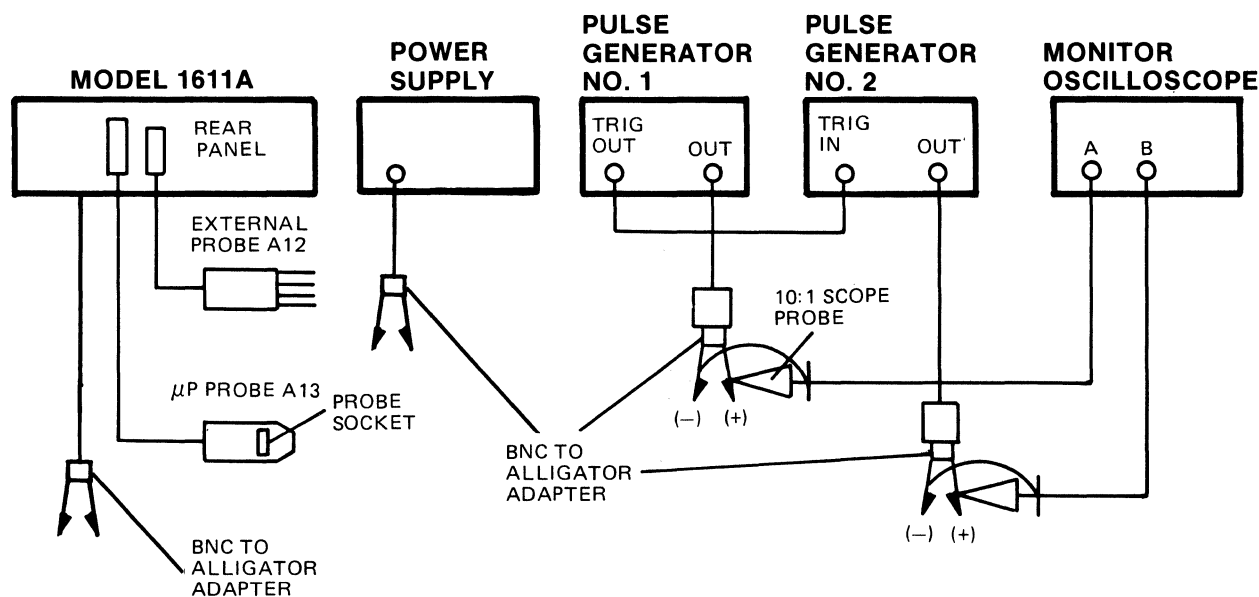


Figure 4-10. Address Lines Test Setup

PROCEDURE:

- Connect test equipment as shown in figure 4-10.
- Connect +5 V from power supply between pin 23 (READY), pin 19 (SYNC) and pin 2 (GND) of microprocessor probe A13 test socket.
- Connect pulse generator No. 1 between pin 15 ($\Phi 2$) and pin 2 (GND) of microprocessor probe A13 test socket.
- Connect pulse generator No. 2 between pin 25 (A0) and pin 2 (GND) of microprocessor probe A13 test socket.
- Adjust pulse generators for waveforms shown in figure 4-11.

PERFORMANCE TESTS

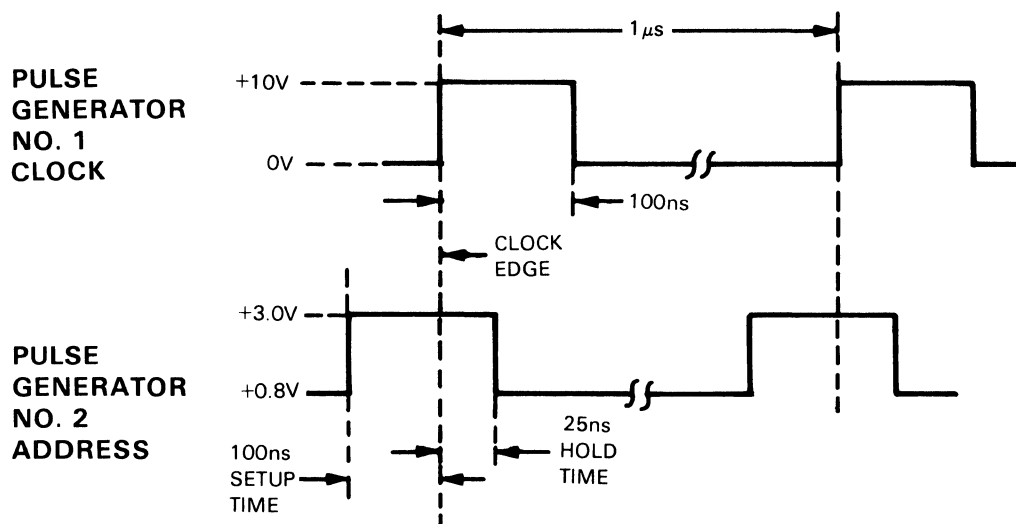


Figure 4-11. Address Lines Test Waveforms

- f. Press TRACE key. Verify that displayed list ADRS field matches that shown in table 4-1 for A₀.
- g. Disconnect pulse generator No. 2 from pin 25 of μ P probe A13.
- h. Repeat steps d through f for each of the remaining ADDRESS lines (A₁ - A₁₅) and verify that the display ADRS field is as shown in table 4-1.

Table 4-1. Address Field Display

Address Line	μ P Probe A13 Socket Pin	ADRS Field
A ₀	25	0001
A ₁	26	0002
A ₂	27	0004
A ₃	29	0008
A ₄	30	0010
A ₅	31	0020
A ₆	32	0040
A ₇	33	0080
A ₈	34	0100
A ₉	35	0200
A ₁₀	1	0400
A ₁₁	40	0800
A ₁₂	37	1000
A ₁₃	38	2000
A ₁₄	39	4000
A ₁₅	36	8000

PERFORMANCE TESTS

4-25. DATA LINES TEST.

SPECIFICATION:

Setup time: ≥ 100 ns relative to rising edge of $\Phi 2$.

Hold time: ≥ 25 ns relative to rising edge of $\Phi 2$.

Threshold: Logic 1 (HI) +3 V to +6 V;

Logic 0 (LO) -1.0 V to +0.8 V.

DESCRIPTION:

A high pulse (logic 1) that satisfies minimum setup time, hold time, and threshold is applied to each data line input and clocked into the 1611A. The READY and SYNC inputs of the μ P probe A13 are connected to +5 V to enable data to be clocked into the 1611A. The CRT display is then checked to verify proper operation of the line under test.

EQUIPMENT:

Pulse Generator (2)	HP 8013B
BNC-to-Alligator Clip Adapter (3)	HP P/N 8120-1292
Power Supply (1)	HP 6213A
Oscilloscope (1)	HP 1740A

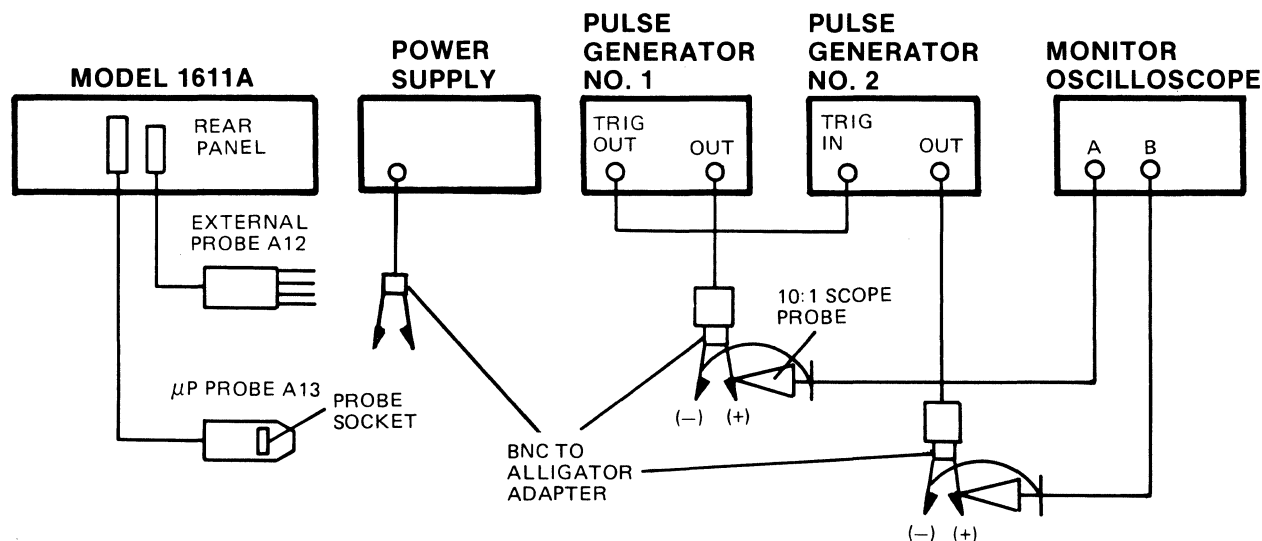


Figure 4-12. Data Lines Test Setup

PROCEDURE:

- Connect test equipment as shown in figure 4-12.
- Connect +5 V from power supply between pin 23 (READY), pin 19 (SYNC) and pin 2 (GND) of microprocessor probe A13 test socket.
- Connect pulse generator No. 1 between pin 15 ($\Phi 2$) and pin 2 (GND) of microprocessor probe A13 test socket.
- Connect pulse generator No. 2 between pin 10 (D0) and pin 2 (GND) of microprocessor probe A13 test socket.
- Adjust pulse generators for waveforms shown in figure 4-13.

PERFORMANCE TESTS

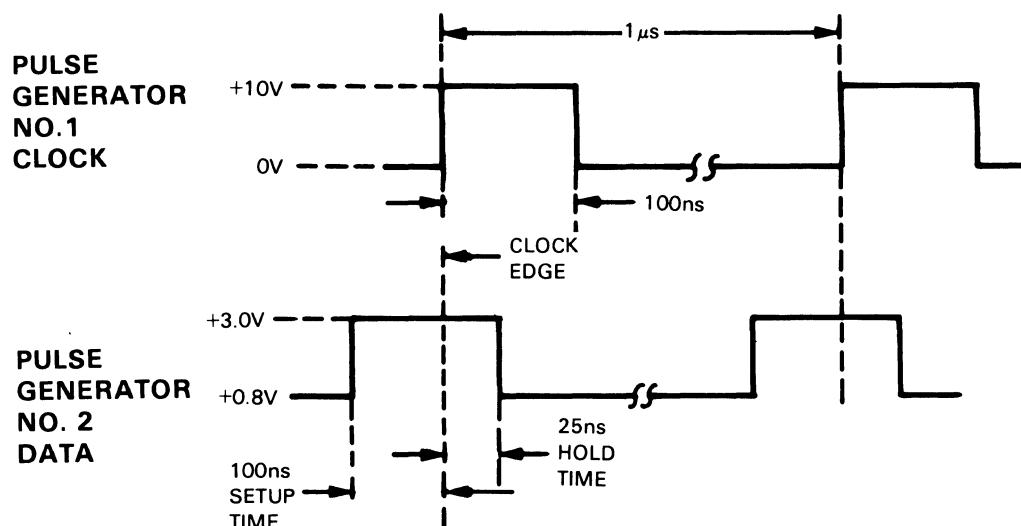


Figure 4-13. Data Lines Test Waveforms

- f. Press TRACE key. Verify that displayed list OPCODE/DATA field matches that shown in table 4-2.

NOTE

It may be necessary to use ABSOLUTE/MNEOMIC key to obtain this display.

- g. Disconnect pulse generator No. 2 from pin 10 of microprocessor probe A13.
- h. Repeat steps d through f for each of the remaining data lines (D_0 - D_7) and verify that the display OPCODE/DATA field is as shown in table 4-2.

Table 4-2. OPCODE/DATA Field Display

Data Line	μ P Probe A13 Socket Pin	OPCODE/DATA Field
D_0	10	01 WRITE
D_1	9	02 READ
D_2	8	04 WRITE
D_3	7	08 WRITE
D_4	3	10 OUTPUT
D_5	4	20 OPCODE
D_6	5	40 OUTPUT
D_7	6	80 WRITE

PERFORMANCE TESTS

4-26. EXTERNAL LINES TEST.

SPECIFICATION:

Setup time: ≥ 250 ns relative to rising edge of $\Phi 2$.

Hold time: ≥ 0 ns relative to rising edge of $\Phi 2$.

Threshold: Logic 1 (HI) +2.4 V to +5.5 V;

Logic 0 (LO) -0.8 V to +0.8 V.

DESCRIPTION:

A high pulse (logic 1) that satisfies minimum setup time, hold time, and threshold is applied to each external probe A12 input and clocked into the 1611A. The READY and SYNC lines are connected to +5 V to enable data to be clocked into the 1611A. The CRT display is checked to verify proper operation.

EQUIPMENT:

Pulse Generator (2)	HP 8013B
BNC-to-Alligator Clip Adapter (3)	HP P/N 8120-1292
Oscilloscope (1)	HP 1740A
Power Supply (1)	HP 6213A

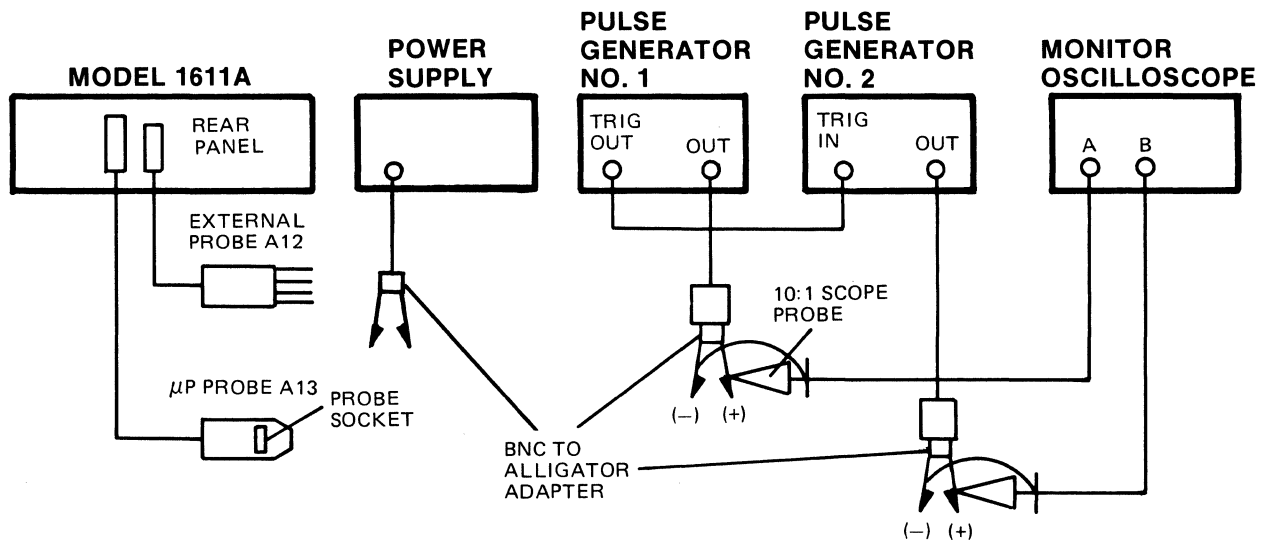


Figure 4-14. External Lines Test Setup

PROCEDURE:

- Connect test equipment as shown in figure 4-14.
- Connect +5 V from power supply between pin 23 (READY), pin 19 (SYNC) and pin 2 (GND) of μ P probe A13 test socket.
- Connect pulse generator No. 1 between pin 15 ($\Phi 2$) and pin 2 (GND) of μ P probe A13 test socket.
- Connect pulse generator No. 2 between EXTERNAL input 0 and GROUND.
- Adjust pulse generators for waveforms shown in figure 4-15.

PERFORMANCE TESTS

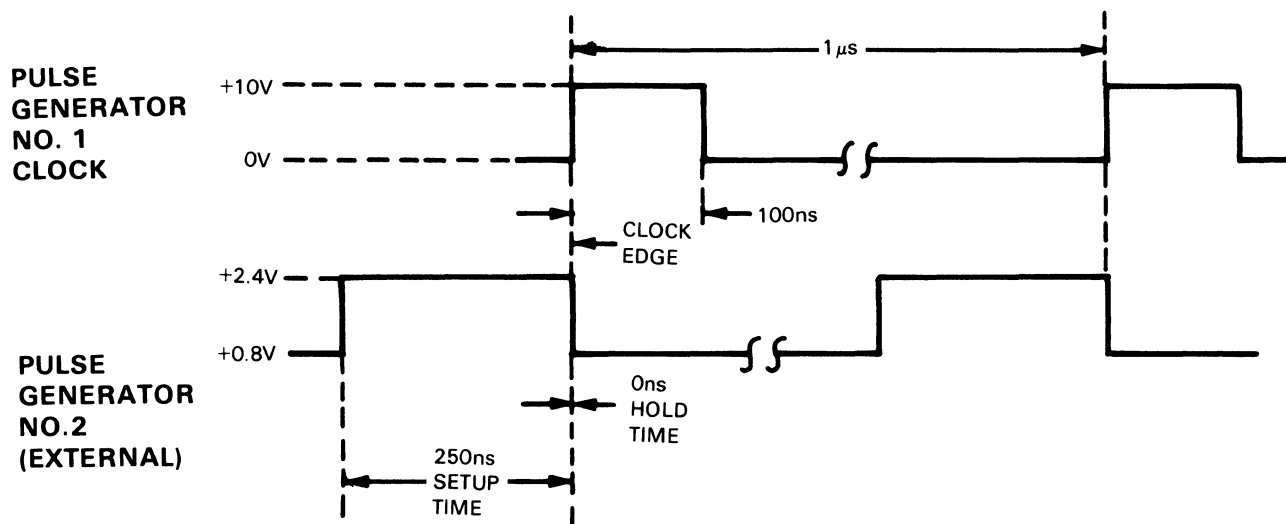


Figure 4-15. External Lines Test Waveforms

- f. Press TRACE key. Verify that displayed EXTERNAL field matches that shown in table 4-3 for external input 0.
- g. Disconnect pulse generator No. 2 from 0 input of external probe A12.
- h. Repeat steps d through g for each of the remaining external probe lines (1 through 7) and verify that the display EXTERNAL field matches table 4-3.

Table 4-3. EXTERNAL Field Display

External Input	EXTERNAL Field
0	0000 0001
1	0000 0010
2	0000 0100
3	0000 1000
4	0001 0000
5	0010 0000
6	0100 0000
7	1000 0000

- i. Disconnect all test equipment from μ P and external probes, A13 and A12.

PERFORMANCE TESTS

4-27. REAR-PANEL OUTPUT TESTS.

SPECIFICATION:

Threshold: Logic 1 (HI) 2.0 V into 50 ohms.
 Logic 0 (LO) +4.0 V into 50 ohms.

DESCRIPTION:

These tests verify that the 1611A produces proper rear-panel outputs.

EQUIPMENT:

Oscilloscope (1)	HP 1740A
50 Ohm Feedthroughs (2)	HP 10100C

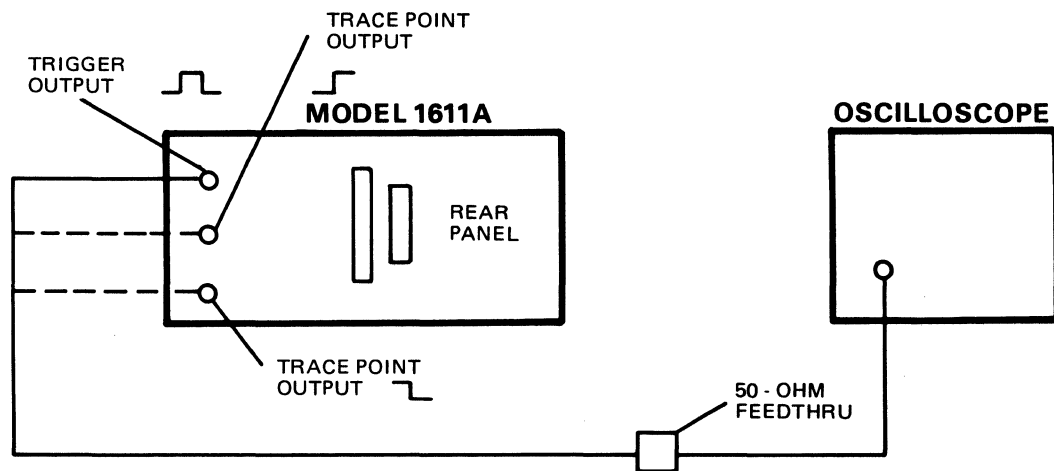


Figure 4-16. Rear-panel Outputs Test Setup

PROCEDURE:
Trigger Output

- a. Plug 40-pin male connector from μ P probe cable into front-panel PROBE TEST socket. (Reconnect probe cable to μ P probe A13 if disconnected.)
- b. Connect TRIGGER OUTPUT to oscilloscope as shown in figure 4-16.
- c. Verify that TRIGGER OUTPUT pulses have maximum amplitude greater than +2.0 V and minimum amplitude less than +0.4 V.

Trace Point $\square$ / $\sqcap$ Output.

- a. Connect TRACE POINT $\square$ output from 1611A rear panel to oscilloscope.
- b. While holding TRACE key down, verify presence of pulses with maximum amplitude greater than +2.0 V and minimum amplitude less than +0.4 V.
- c. Repeat steps a and b for TRACE POINT $\sqcap$.

PERFORMANCE TEST RECORD**HEWLETT-PACKARD****MODEL 1611A Option A80****LOGIC ANALYZER**

Tested by _____

Serial No. _____

Date _____

Paragraph Number	Test	Specifications	Passed	Failed
9	Clock	$0 \leq +0.8 \text{ V}$, $1 \geq +9.0 \text{ V}$, 75 ns min (high or low)	_____	_____
10	INTE	$0 \leq +0.8 \text{ V}$, $1 \geq +3.0 \text{ V}$	_____	_____
11	HLDA	$0 \leq +0.8 \text{ V}$, $1 \geq +3.0 \text{ V}$	_____	_____
12	WAIT	$0 \leq +0.8 \text{ V}$, $1 \geq +3.0 \text{ V}$	_____	_____
13	READY	$0 \leq +0.8 \text{ V}$, $1 \geq +3.0 \text{ V}$, Setup $\geq 80 \text{ ns}$ Hold $\geq 0 \text{ ns}$	_____	_____
14	SYNC	$0 \leq +0.8 \text{ V}$, $1 \geq +3.0 \text{ V}$, Setup $\geq 100 \text{ ns}$ Hold $\geq 25 \text{ ns}$	_____	_____
15	Data Lines D ₀ - D ₇	$0 \leq +0.8 \text{ V}$, $1 \geq +3.0 \text{ V}$, Setup $\geq 100 \text{ ns}$ Hold $\geq 25 \text{ ns}$	_____	_____
16	Address Lines A ₀ - A ₁₅	$0 \leq +0.8 \text{ V}$, $1 \geq +3.0 \text{ V}$, Setup $\geq 100 \text{ ns}$ Hold $\geq 25 \text{ ns}$	_____	_____
17	External Inputs 0-7	$0 \leq +0.8 \text{ V}$, $1 \geq +2.4 \text{ V}$, Setup $\geq 250 \text{ ns}$ Hold $\geq 0 \text{ ns}$	_____	_____
19	Trigger Output	$0 \leq +0.4 \text{ V}$, $1 \geq +2.0 \text{ V}$ into 50 Ω	_____	_____
20	Trace Points Outputs	$0 \leq +0.4 \text{ V}$, $1 \geq +2.0 \text{ V}$ into 50 Ω	_____	_____

SECTION V

ADJUSTMENTS

There are no adjustments on the Model 10258B/1611A Option A80.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. Table 6-1 lists all replaceable parts for the Model 10258B/1611A Option A80. Replaceable parts are listed in reference designator order.

Table 6-1. Replaceable Parts

Reference Designation	HP Part No.	Qty	Description	Mfr Code	Mfr Part No.
A9	01611-66531	1	BOARD ASSEMBLY, OPTION A80 PERSONALITY	28480	01611-66531
A10	01611-66570		BOARD ASSEMBLY, OPTION A80 ROM	28480	01611-66570
A11	01611-68706		ASSEMBLY, OPTION A80 PERSONALITY PANEL	28480	01611-68706
A13	01611-62107		ASSEMBLY, A80 MICROPROCESSOR PROBE	28480	01611-62107
MP1	1540-0325		CASE, CRYG HANDLE	28480	1540-0325
A9	01611-66531	1	BOARD ASSEMBLY, OPTION A80 PERSONALITY	28480	01611-66531
A9C1	0180-0229	1	CAPACITOR-FXD 33UF 10V TA	28480	0180-0229
A9C2	0160-2055	4	CAPACITOR-FXD .01UF 100V CER	28480	0160-2055
A9C3	0160-2202	1	CAPACITOR-FXD 75PF 300V MI	28480	0160-2202
A9C4	0160-3449	1	CAPACITOR-FXD 2000PF 250V CER	28480	0160-3449
A9C5	0160-2055	1	CAPACITOR-FXD .01UF 100V CER	28480	0160-2055
A9C6	0160-2055		CAPACITOR-FXD .01UF 100V CER	28480	0160-2055
A9C7	0180-0197		CAPACITOR-FXD 2.2UF 20V TA	28480	0180-0197
A9C8	0160-2055		CAPACITOR-FXD .01UF 100V CER	28480	0160-2055
A9C9	0160-2306		CAPACITOR-FXD 27PF 300V MI	28480	0160-2306
A9C10	0160-2306	2	CAPACITOR-FXD 27PF 300V MI	28480	0160-2306
A9R1	0757-0442		RESISTOR-FXD 10K .12MF	24546	CR-118-TO-1002-F
THRU		1			
A9R4					
A9R5	0757-0438		RESISTOR-FXD 5.11K .12MF	28480	0757-0438
A9R6	0757-0442		RESISTOR-FXD 10K .12MF	24546	CR-118-TO-1002-F
A9R7	0757-0442		RESISTOR-FXD 10K .12MF	24546	CR-118-TO-1002-F
A9R8	0757-0730	1	RESISTOR-FXD 750 .25MF	28480	0757-0730
A9R9	0684-2711	1	RESISTOR-FXD 270 .25CC	28480	0684-2711
A9R10	0757-0415	2	RESISTOR-FXD 475 .12MF	28480	0757-0415
A9R11	0757-0415	1	RESISTOR-FXD 475 .12MF	28480	0757-0415
A9J2	1251-3024		CONNECTOR 26-PIN MALE RECTANGULAR	04726	3429-2002
A9U1	1810-0283	2	NETWORK-RES 16-PIN-DIP 270	01607	316B271
A9U2	1820-0661	1	IC SN7432N TTL QUAD 2 OR	01295	SN7432N
A9U3	1820-1464	1	IC SN74393N TTL DUAL 4-BIT BIN COUNTER	01295	SN74393N
A9U4	1820-1144	1	IC SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A9U5	1820-1195	8	IC SN74LS175N TTL LS QUAD D F-F	01295	SN74LS175N
A9U6	1820-1204	1	IC SN74LS20N TTL LS DUAL 4-NAND	01295	SN74LS20N
A9U7	1820-1217	1	IC SN74LS151N TTL LS 1-OF-8 DATA SEL/MUX	01295	SN74LS151N
A9U8	1810-0283	2	NETWORK-RES 16-PIN-DIP 270	01607	316B271
A9U9	1820-1112		IC SN74LS74N TTL LS DUAL D F-F	01295	SN74LS74N
A9U10	1820-1197	2	IC SN74LS00N TTL LS QUAD 2-NAND	01295	SN74LS00N
A9U11	1820-1322	1	IC SN74S02N TTL L QUAD 2-NOR	01295	SN74S02N
A9U12	1820-0514	1	IC SN7426N TTL QUAD 2-NAND	01295	SN7426N
A9U13	1820-0077	1	IC SN7474N TTL DUAL D F-F	01295	SN7474N
A9U14	1820-1112	1	IC SN74LS74N TTL LS DUAL D F-F	01295	SN74LS74N
A9U15	1820-0579		IC SN74123N TTL DUAL MONO MV	01295	SN74123N
A9U16	1820-1197	1	IC SN74LS00N TTL LS QUAD 2-NAND	01295	SN74LS00N
A9U17	1820-1195		IC SN74LS175N TTL LS QUAD D F-F	01295	SN74LS175N
THRU		1			
A9U23					
A10	01611-66570	1	BOARD ASSEMBLY, OPTION A80 ROM	28480	01611-66570
A10C1	0180-0228	1	CAPACITOR-FXD 22UF 15V TA	56289	150D226X901582
A10C2	0160-3443	1	CAPACITOR-FXD .1UF 50V CER	02813	CY20C104Z2
A10C3	0160-2055	4	CAPACITOR-FXD .01UF 100V CER	28480	0160-2055
THRU		2			
A10C6					
A10R1	0757-0904		RESISTOR-FXD 150 2% .125W	07716	CEA-993
A10U1	1820-1195		IC SN 74LS175N TTL LS QUAD D F-F	01295	SN74LS175N
A10U2	1820-1195		IC SN 74LS175N TTL LS QUAD D F-F	01295	SN74LS175N
A10U3	1820-1208	1	IC SN 74LS32N TTL LS QUAD 2-OR	01295	SN74LS32N
A10U4	1820-1917	1	IC SN 74LS240N TTL LS OCTAL 3-STATE BUFF	01295	SN74LS240N
A10U5		1	NOT USED IN OPTION A80		
THRU					
A10U7					
A10U8	1816-1147		IC MEMORY	28480	1816-1147
A10U9	1818-0707		IC MEMORY	28480	1818-0707
A10U10	1818-0711	1	IC MEMORY	28480	1818-0711
A10U11	1820-1216	1	IC SN74LS138N TTL LS 3-TO-8 LINE DEC/MUX	01295	SN74LS138N
A10U12	1810-0055	1	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG 10K	28480	1810-0055
A10XU8	1200-0622	3	SOCKET-IC 24-PIN-DIP	28480	1200-0622
A10XU9	1200-0622		SOCKET-IC 24-PIN-DIP	28480	1200-0622
A10XU10	1200-0622		SOCKET-IC 24-PIN-DIP	28480	1200-0622
A11	01611-68706	1	ASSEMBLY, OPTION A80 PERSONALITY PANEL	28480	01611-68706
A11H1	2200-0103	4	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZ1	28480	2200-0103

Table 6-1. Replaceable Parts (Cont'd)

Reference Designation	HP Part No.	Qty	Description	Mfr Code	Mfr Part No.
A11MP1	01611-00208	1	PANEL-A80 AUX DSP	28480	01611-00208
A11MP2	5040-0565	1	BEZEL, CONNECTOR	28480	5040-0565
A11A1	01611-66533	1	PANEL, PERSONALITY A80	28480	01611-66533
A11A1DS1	1990-0486	6	LED-VISIBLE RED LUM-INT=1 MCD IF=20MA-MAX	28480	1990-0486
THRU					
A11A1DS6					
A11A1DS7	1990-0487	1	LED-VISIBLE YEL LUM-INT=1 MCD IF=20MA-MAX	28480	1990-0487
A11A1J1	1200-0623	1	CONNECTOR 40-PIN FEM ZIF	28480	1200-0623
A11A1R1	0684-3311	1	RESISTOR-FXD 330 .25CC	28480	0684-3311
A11A1R2	0684-1021	1	RESISTOR-FXD 1K .25CC	28480	0684-1021
A11A1R3	0757-0280	1	RESISTOR-FXD 1K .12MF	28480	0757-0280
A11A1R4	0757-0409	1	RESISTOR-FXD 274 .12MF	28480	0757-0409
A11A1S1	3101-2119	1	SWITCH-TGL SUBMIN DPDT NS 2A 250VAC	28480	3101-2119
A11A1S2	3101-2118	1	SWITCH-TGL SUBMIN SPDT NS 2A 250VAC	28480	3101-2118
A11A1S3	3101-2214	4	SWITCH-TGL SUBMIN DPDT NS 2A 250VAC	28480	3101-2214
THRU					
A11A1S6					
A11A1VR1	1902-3092	1	VOLTAGE REGULATOR 4.99V	28480	1902-3092
A11A1W1	01611-61605	1	CABLE ASSEMBLY, PERSONALITY (NSR)	28480	01611-61605
A11A1W2	01611-61615	1	CABLE ASSEMBLY, PERSONALITY (NSR)	28480	01611-61615
A13	01611-62107	1	ASSEMBLY, A80 MICROPROCESSOR PROBE	28480	01611-62107
A13A1	01611-66534	1	BOARD ASSEMBLY	28480	01611-66534
A13H1	0624-0306	3	SCREW-THREADED 2-28 .5-IN-LG PAN-HD-POZI	28480	0624-0306
A13H2	0624-0390	2	SCREW-THREADED 2-28 .625-IN-LG PAN-HD-POZI	28480	0624-0390
A13MP1	5040-8126	1	PROBE POD-BOTTOM	28480	5040-8126
A13MP2	01611-24102	1	PROBE POD-TOP	28480	01611-24102
A13MP3	7120-6804	1	LABEL-PROBE 8080	28480	7120-6804
A13MP4	1540-0440	1	CASE-CARRYING	28480	1540-0440
A13W1	01611-61609	1	CABLE ASSEMBLY, TEST CLIP (NOT SUPPLIED WITH A13. ORDER SEPARATELY)	28480	01611-61609
A13W1	01611-61610	1	CABLE ASSEMBLY, DIP-LONG	28480	01611-61610
A13W1	01611-61612	1	CABLE ASSEMBLY, DIP-SHORT (NOT SUPPLIED WITH A13. ORDER SEPARATELY)	28480	01611-61612
A13W2	01611-61623	1	CABLE ASSEMBLY-MICROPROCESSOR PROBE	28480	01611-61623
A13W2H1	2200-0111	2	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	28480	2200-0111
A13W2H2	3050-0235	2	WASHER-FL MTLCL NO. 4 .117-IN-ID	28480	3050-0235
A13W2H3	2190-0019	2	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
A13W2H4	2260-0002	2	NUT-HEX-DBL-CHAM 4-40-THD .062-7HK	28480	2260-0002
A13W2MP1	01611-61201	1	CLAMP, CABLE	28480	01611-61201
A13A1C1	0160-2253	1	CAPACITOR-FXD 6.8PF 500V CER	28480	0160-2253
A13A1C2	0180-0155	1	CAPACITOR-FXD 2.2UF 20V TA	28480	0180-0155
A13A1C3	0160-2055	2	CAPACITOR-FXD .01UF 100V CER	28480	0160-2055
A13A1C4	0160-3508	2	CAPACITOR-FXD 1UF 50V CER	28480	0160-3508
A13A1C5	0160-3508	2	CAPACITOR-FXD 1UF 50V CER	28480	0160-3508
A13A1C6	0160-2055	2	CAPACITOR-FXD .01UF 100V CER	28480	0160-2055
A13A1R1	0757-0280	9	RESISTOR-FXD 1K .12MF	28480	0757-0280
THRU					
A13A1R4					
A13A1R5	0757-0441	1	RESISTOR-FXD 8.25K .12MF	28480	0757-0441
A13A1R6	0757-0435	1	RESISTOR-FXD 3.92K .12MF	28480	0757-0435
A13A1R7	0757-0280		RESISTOR-FXD 1K .12MF	28480	0757-0280
A13A1R8	0757-0394	1	RESISTOR-FXD 51.1K .12MF	28480	0757-0394
A13A1R9	0757-0280		RESISTOR-FXD 1K .12MF	28480	0757-0280
THRU					
A13A1R12					
A13A1J1	1200-0623	1	CONNECTOR 40-PIN FEM ZIF	28480	1200-0623
A13A1J2	1251-3782	1	CONNECTOR 40-PIN MALE RECTANGULAR	76381	3432-1002
A13A1U1	1820-1817	5	IC 8T37 HEX BUS RCVR	18324	8T37
THRU					
A13A1U5					
A13A1U6	1820-1198	1	IC SN74LS03N TTL LS OC QUAD 2-NAND	01295	SN74LS03N
A13A1U7	1810-0284	3	NETWORK-RES 16-PIN-DIP 1K	01121	316B102
THRU					
A13A1U9					
A13A1S1	3101-0973	1	SWITCH-SLIDE DPDT-NS .5A 125 VAC	79727	GF126-0018

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual to options for which the content does not apply directly.

7-3. MANUAL CHANGES.

7-4. To adapt this manual to your option, refer to table 7-1 and make all of the manual changes listed opposite your option serial number. Perform these changes in the sequence listed.

7-5. If your option serial number is not listed on the title page of this manual or in table 7-1 below, it may be documented in the yellow MANUAL CHANGES supplement.

Table 7-1. Manual Changes by Serial Prefix Number

Serial Prefix Number	Make Manual Change
1818A and non serialized	1

7-6. MANUAL CHANGE INSTRUCTIONS.

CHANGE 1

ROM Board A10:

Delete: A10 ROM Opt A80, HP Part No. 01611-66570.

Add: A10 ROM Opt A80, HP Part No. 01611-66532.

Table 6-1:

A9U8: Change Reference Designation to A9U6.

Add: A9U7, HP Part No. 1816-1108.

Add: A9U8, HP Part No. 1816-1109.

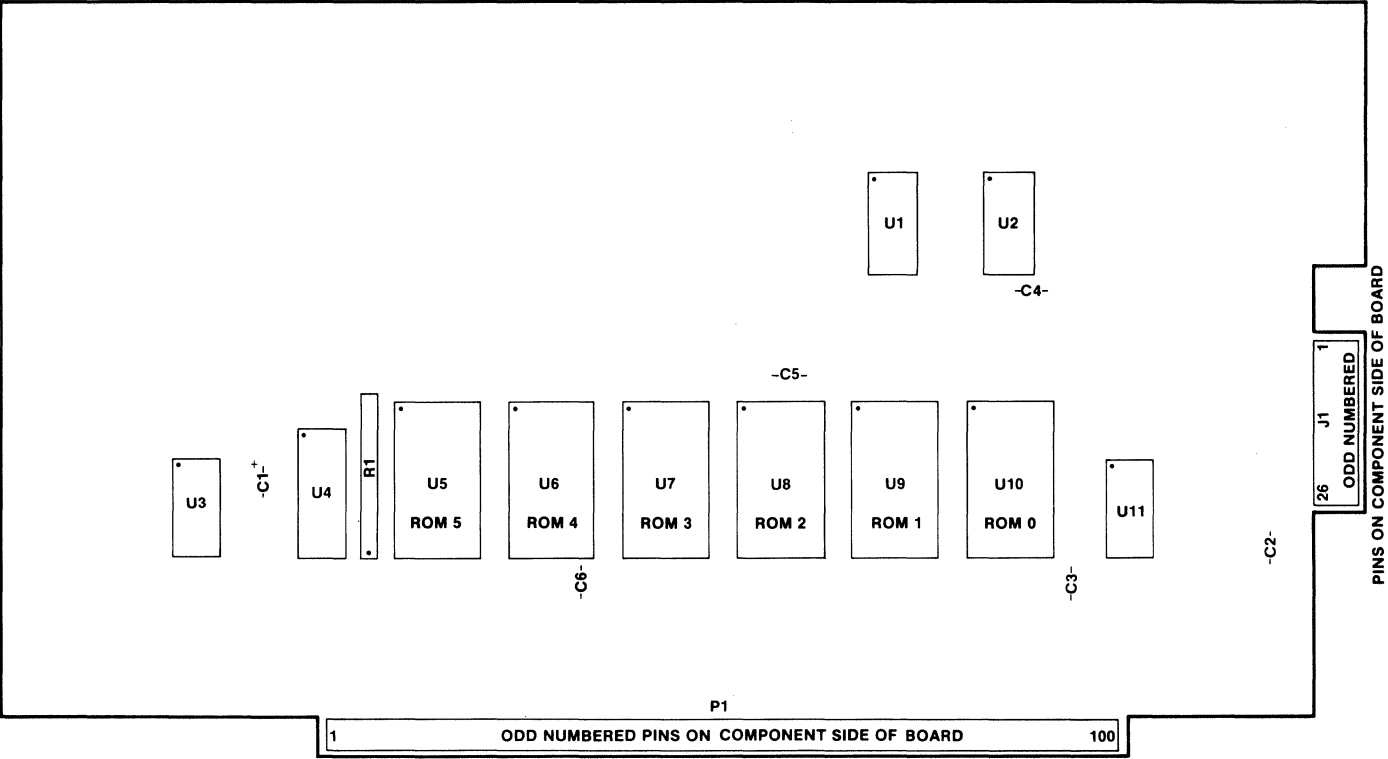
A9U9: Change to HP Part No. 1816-1114.

A9U10: Change to HP Part No. 1816-1112.

Add: XU6-7, HP Part No. 1200-0622, Socket IC 24-Pin-DIP.

Figure 8-4:

Service Sheet 4: Replace with figure 7-1 (2 sheets).



Replacement for Figure 8-2, Service Sheets 2A-B (Sheet 1 of 4)

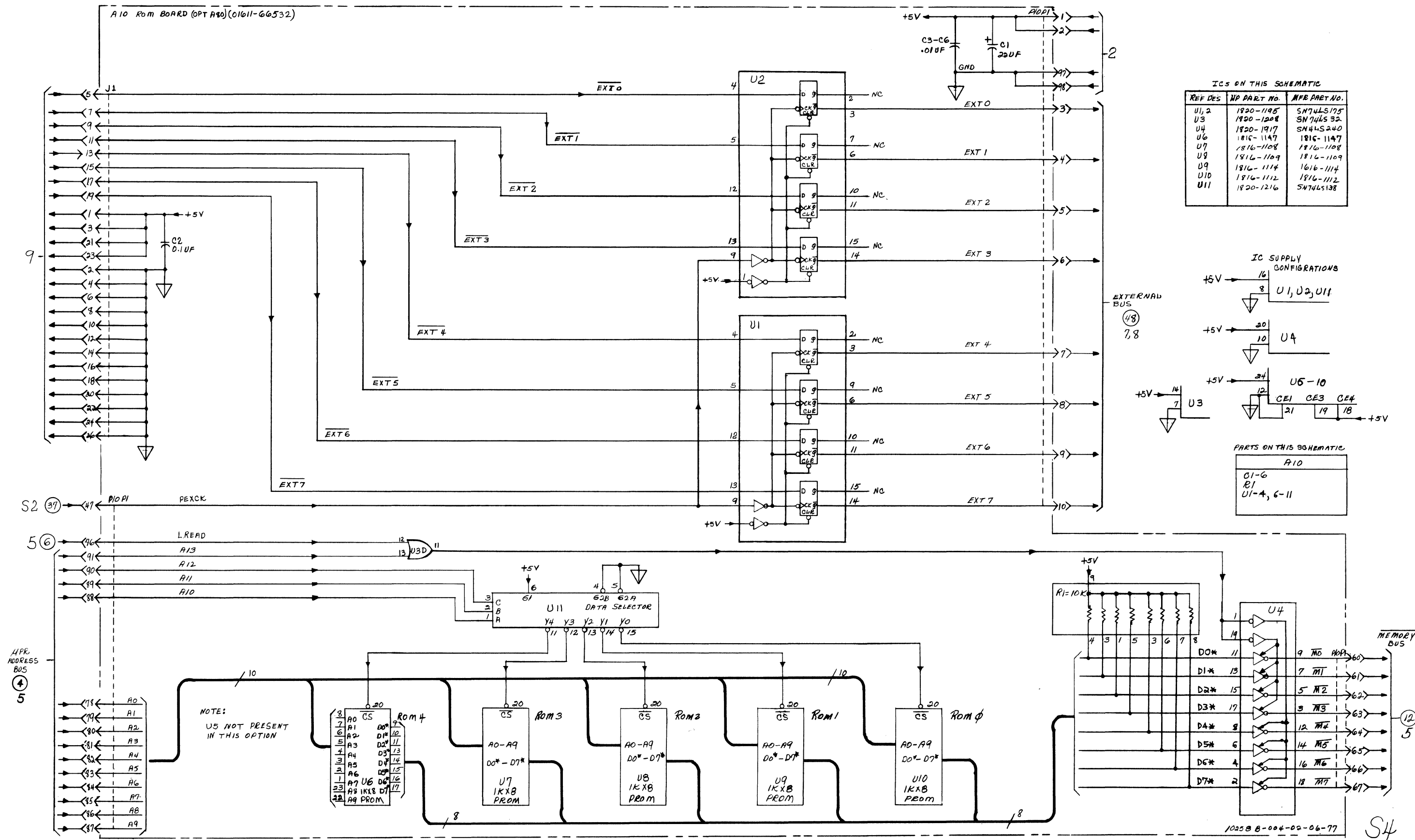


Figure 7-1.
Replacement for Figure 8-4, Service Sheet 4
7-3/(7-4 blank)

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains schematic diagrams for the Model 10258B/1611A Option A80 as well as a signature analysis troubleshooting procedure for service sheet 4.

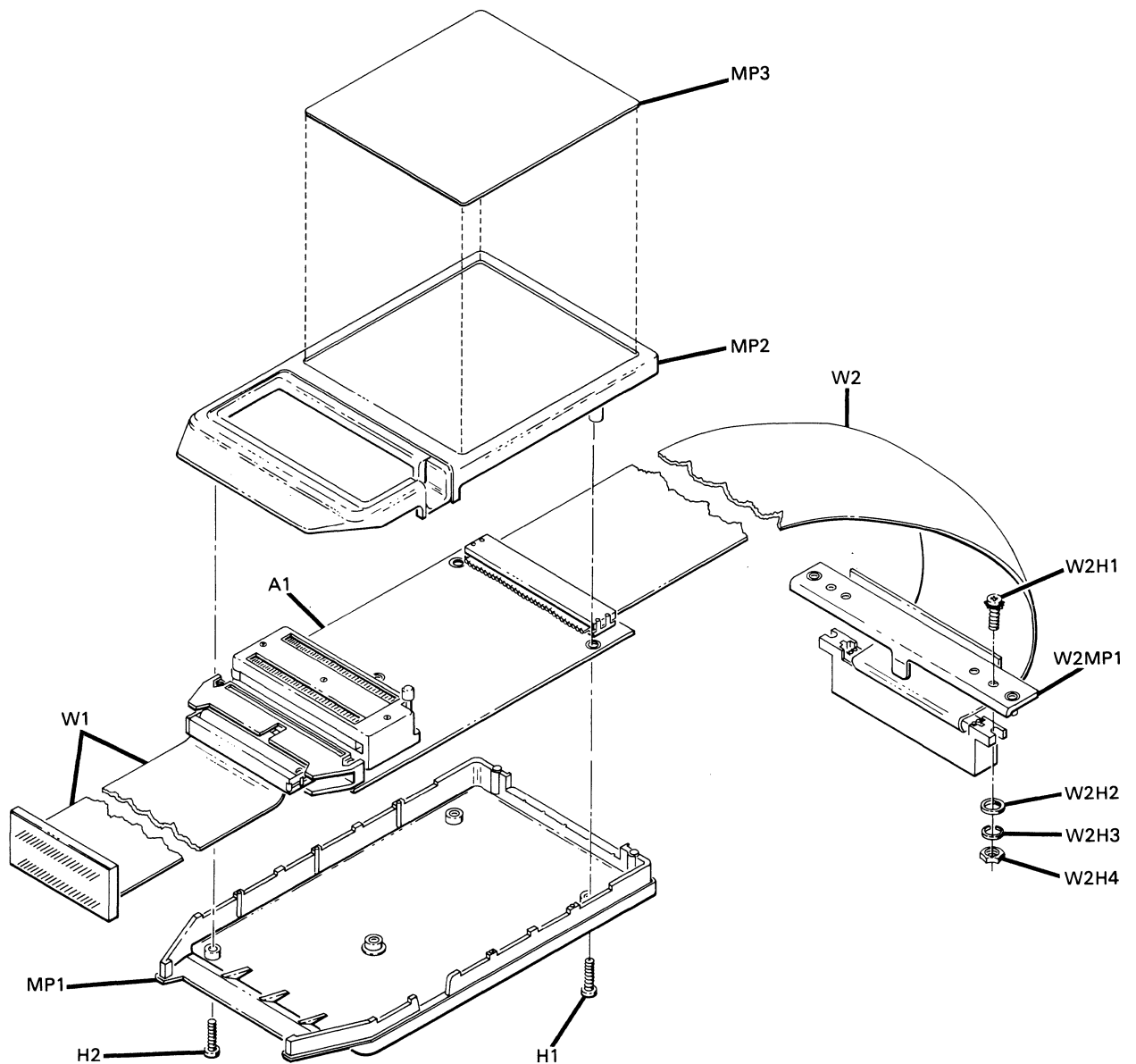
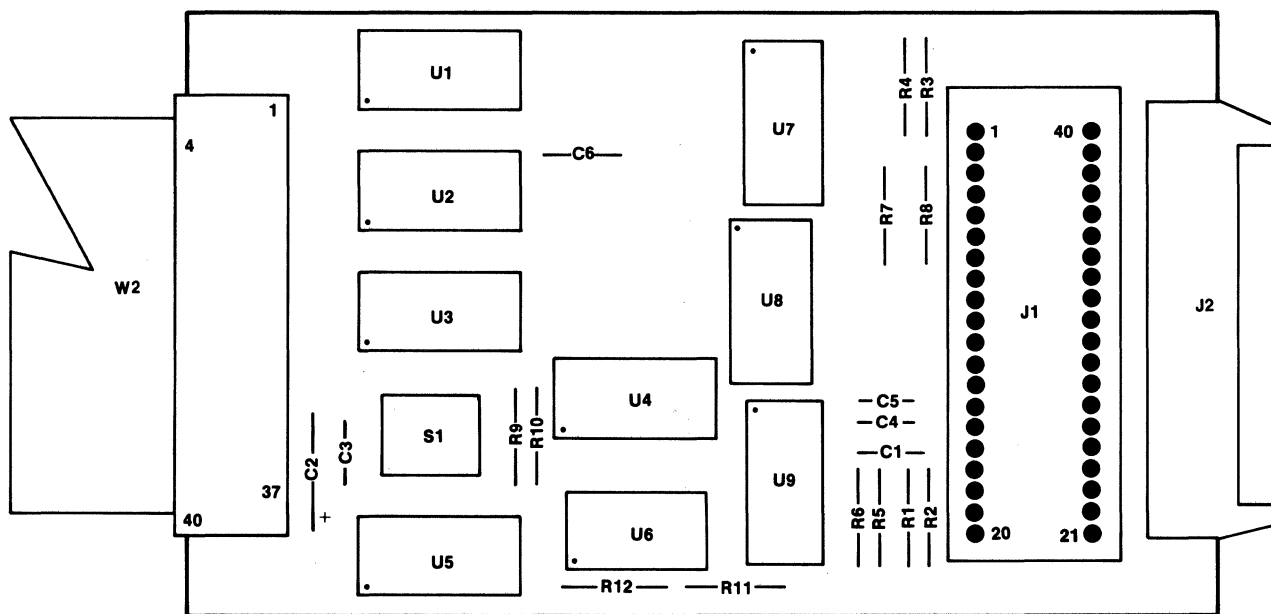


Figure 8-1. Service Sheet 1, Microprocessor Probe A13 (Sheet 1 of 3)



A13A1 Component Location (01611-66534)

Figure 8-1. Service Sheet 1, Microprocessor Probe A13 (Sheet 2 of 3)

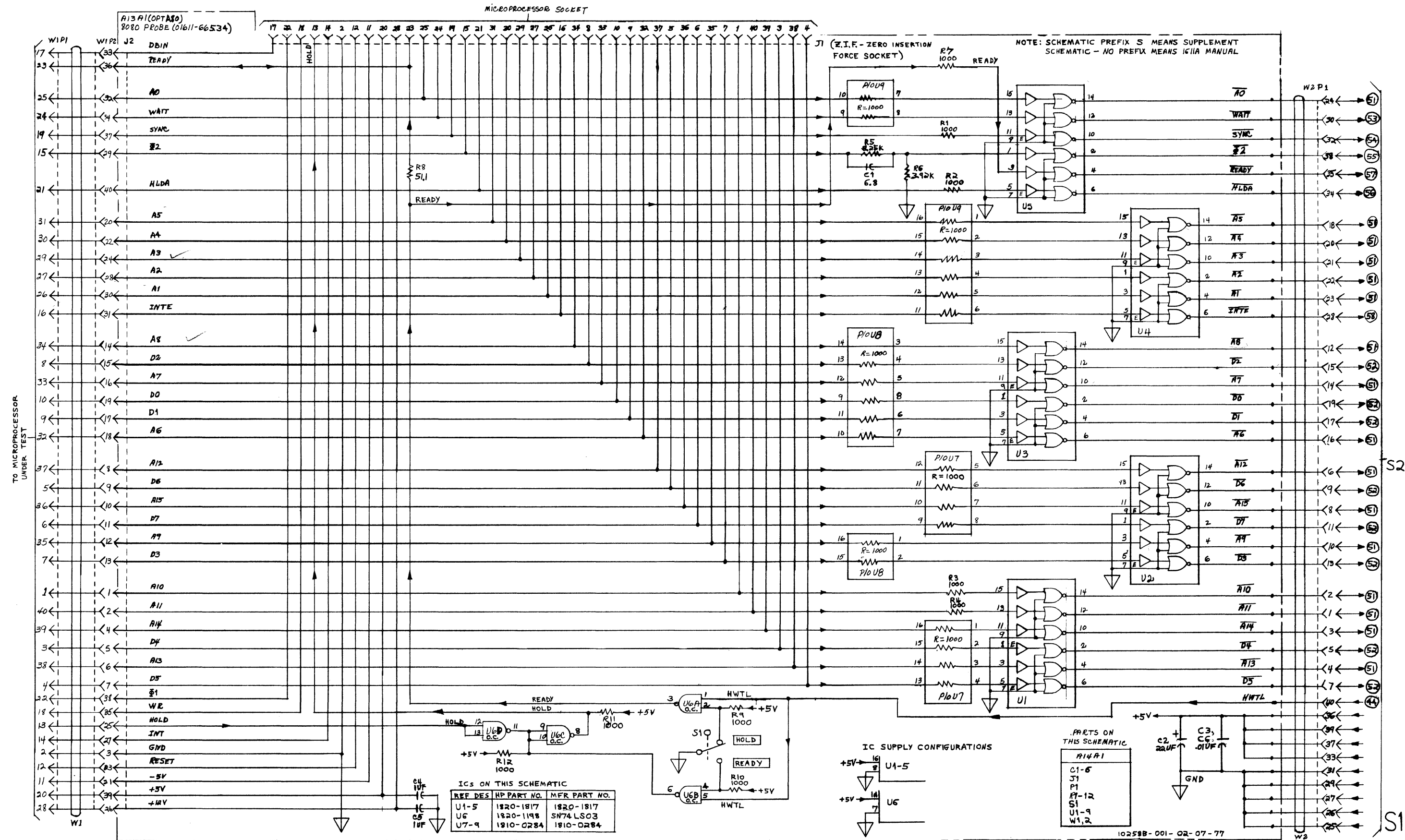
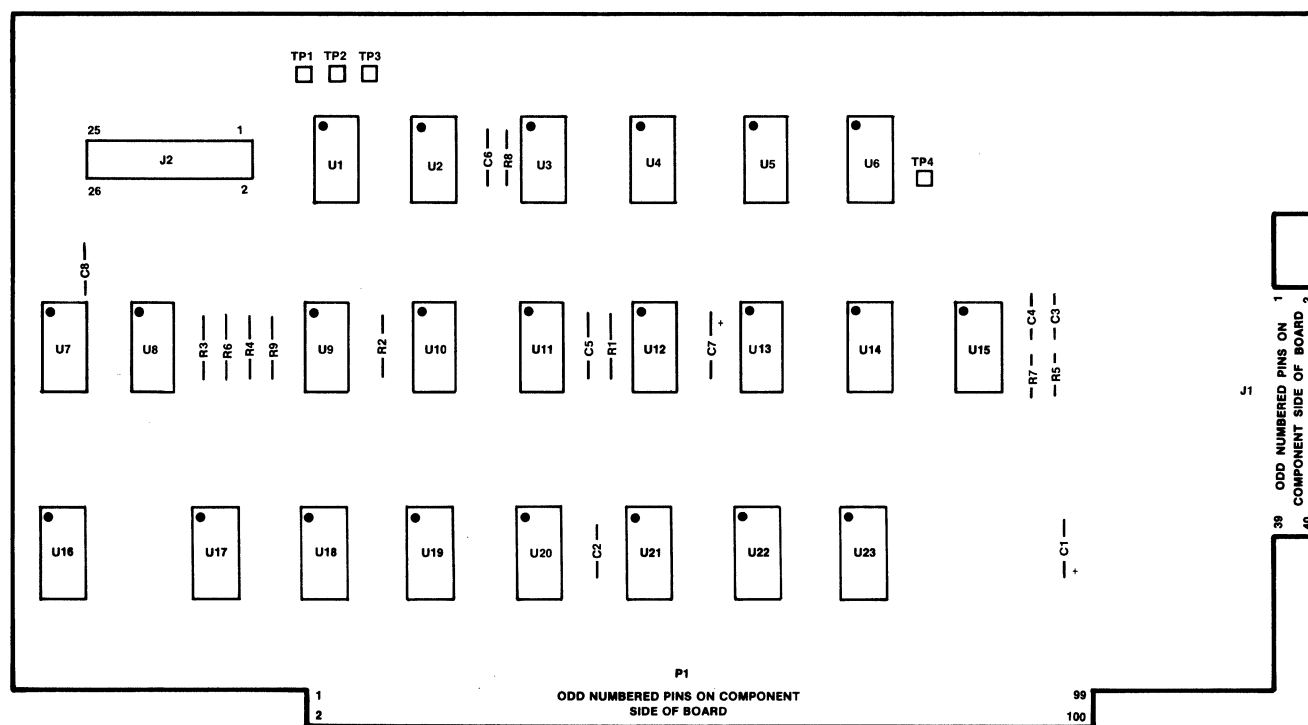


Figure 8-1.
Service Sheet 1, Microprocessor Probe A13 (Sheet 3 of 3)
8-3



A9 Component Location (01611-66531)

Figure 8-2. Service Sheet 2, Personality Board A9 (Sheet 1 of 3)

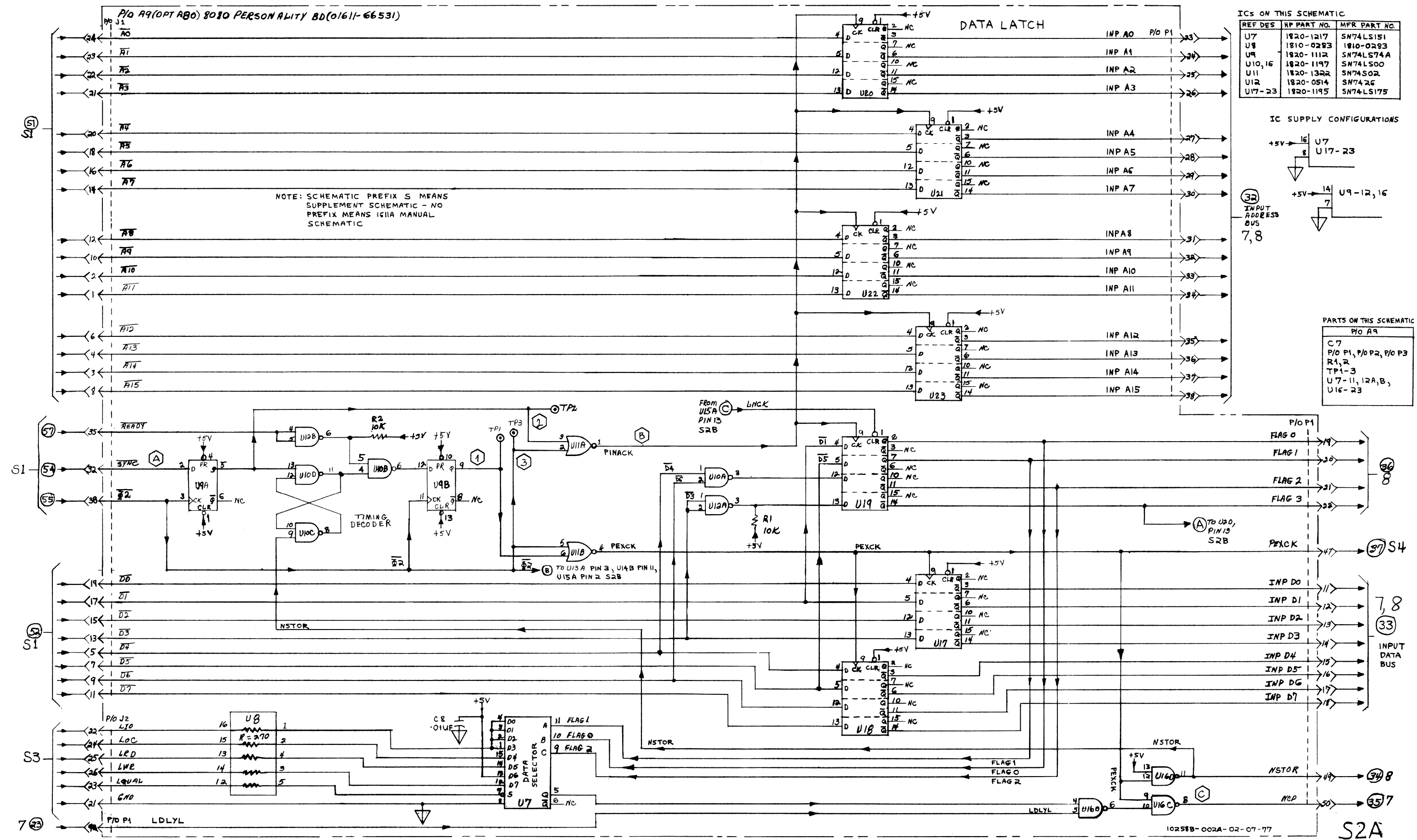


Figure 8-2.
Service Sheet 2, Personality Board A9 (Sheet 2 of 3)
8-5/(8-6 blank)

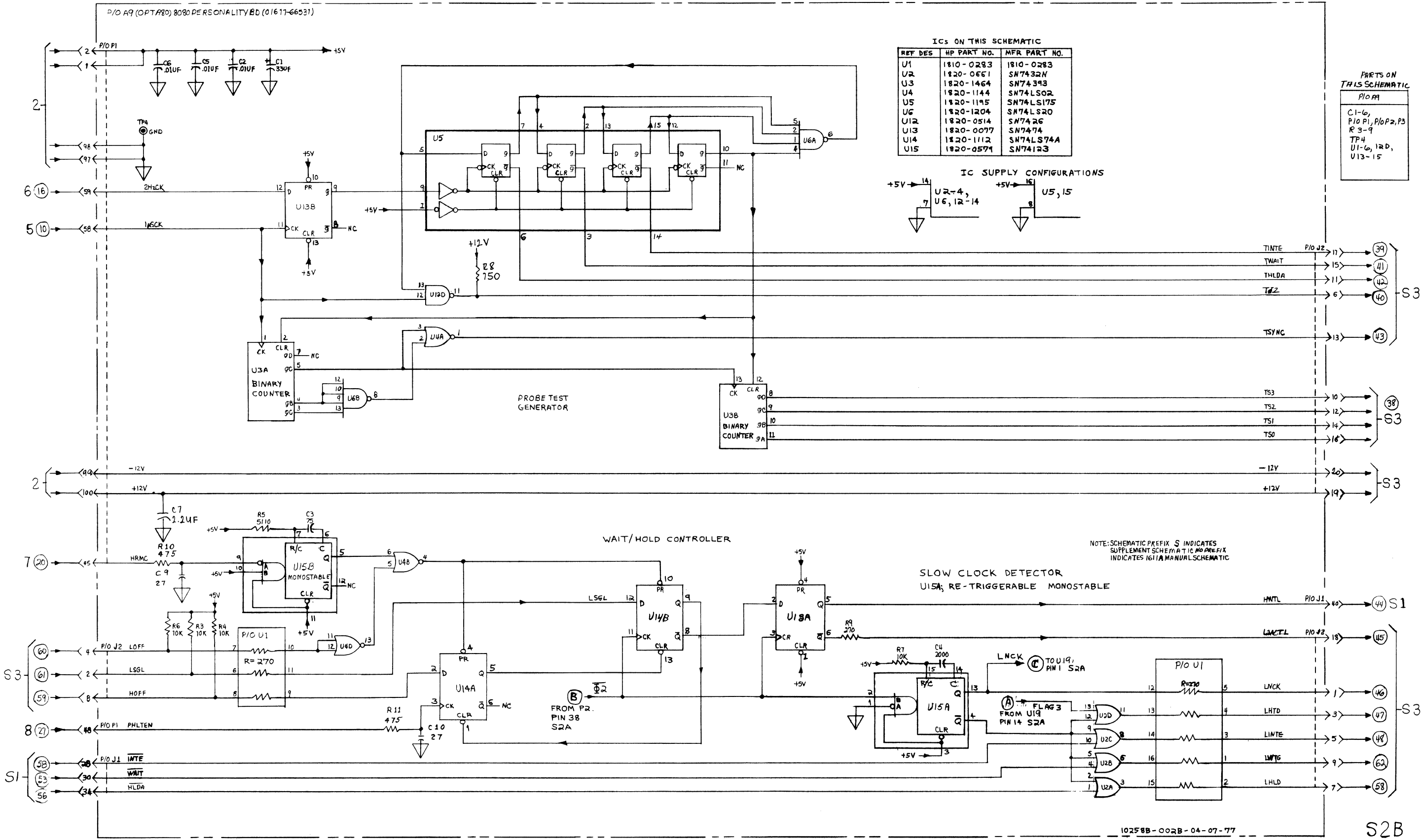
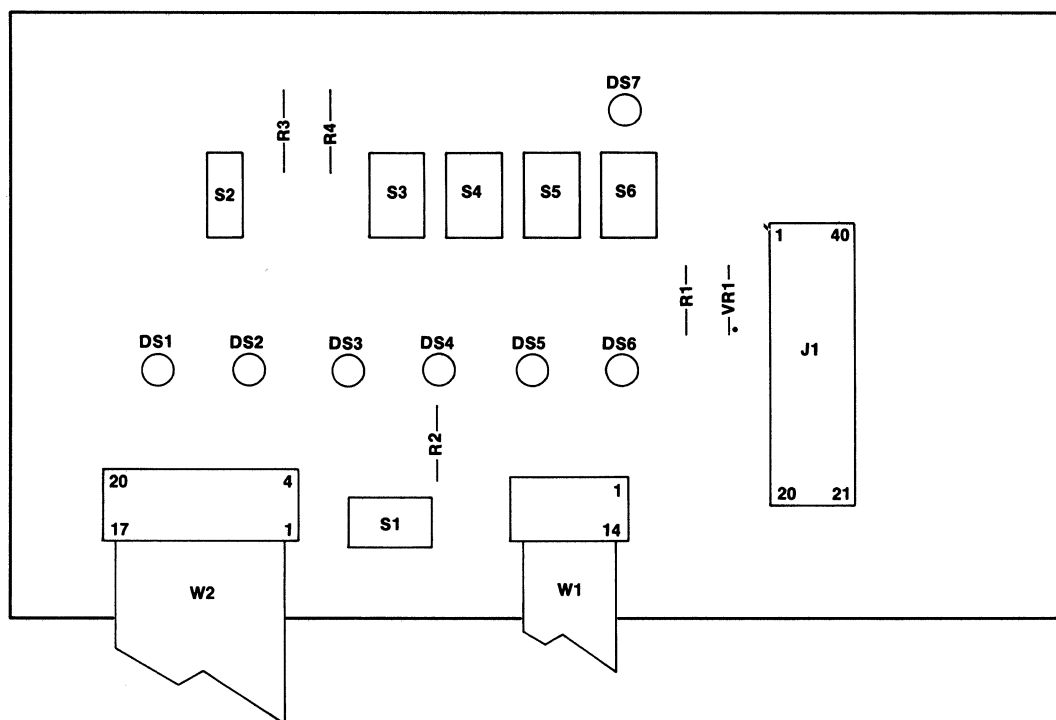


Figure 8-2.
Service Sheet 2, Personality Board A9 (Sheet 3 of 3)
8-7



A11 Component Location (01611-68706)

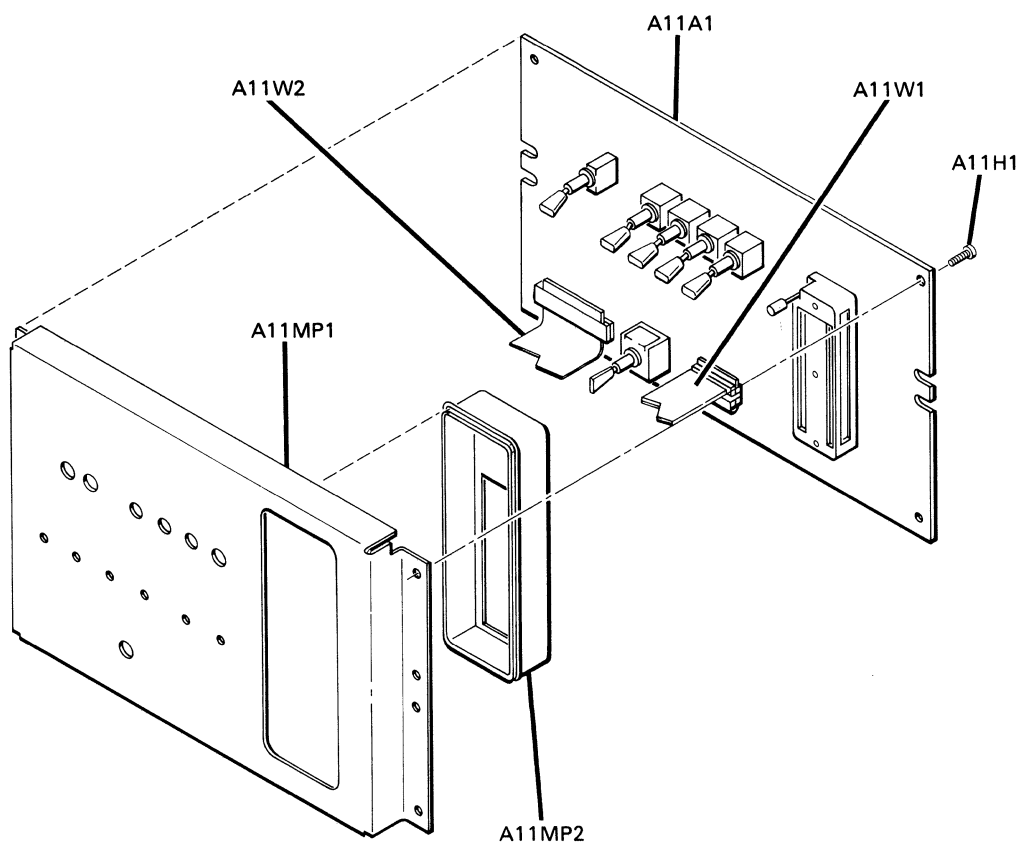


Figure 8-3. Service Sheet 3, Personality Panel A11 (Sheet 1 of 2)

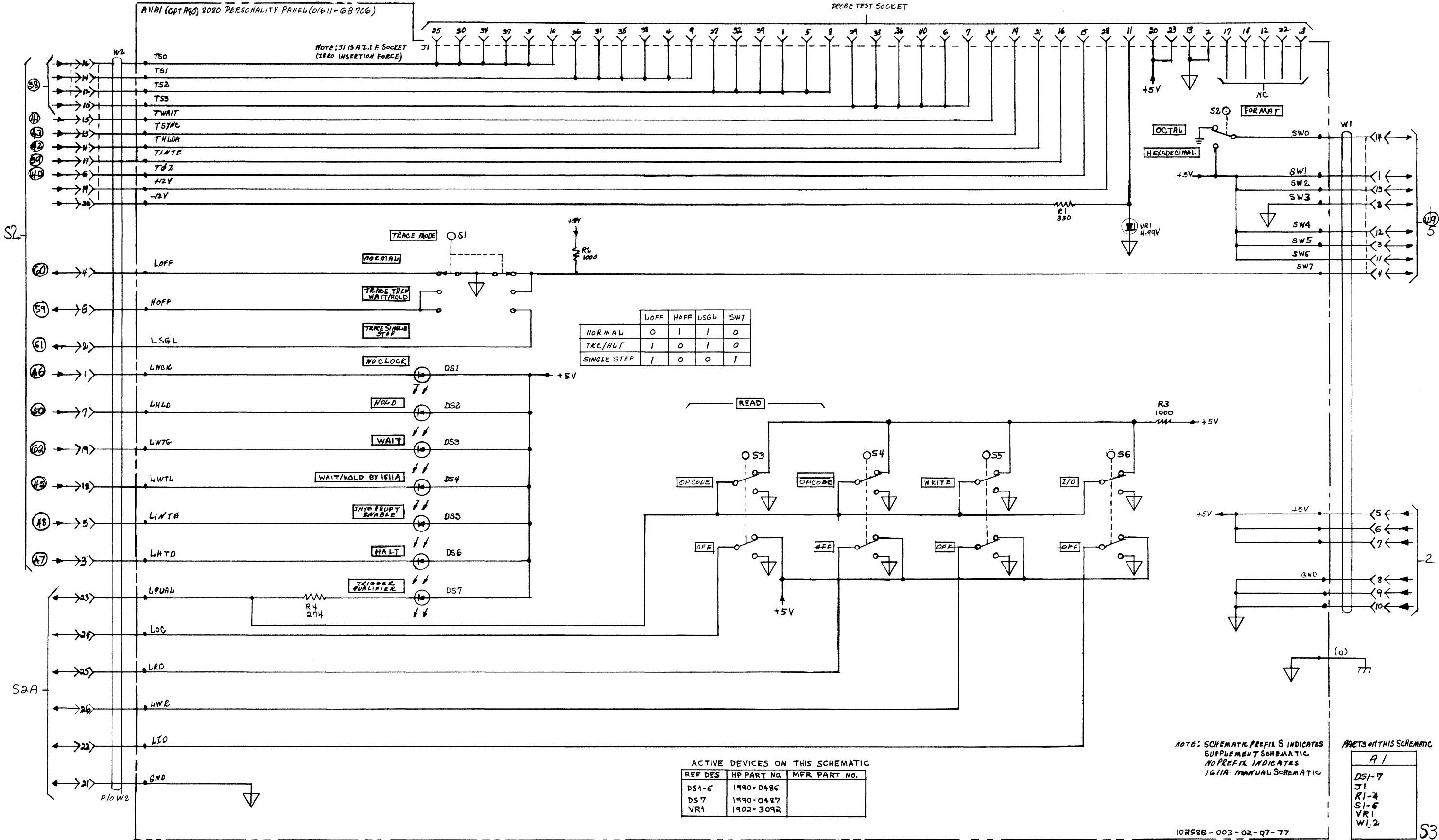


Figure 8-3.
Service Sheet 3, Personality Panel A11 (Sheet 2 of 2)
8-9

SERVICE SHEET 4.

TROUBLESHOOTING.

An HP 5004A Signature Analyzer may be used to troubleshoot the ROM board in a 1611A/Option A80. Follow the ROM Test Troubleshooting Tree. The boxed measurement numbers (101, 102, etc.) shown in the troubleshooting tree are the measurement numbers used in the table of signatures below. To check a measurement, connect the signature analyzer and read the signature at each listed test point.

The arrangement of test No. 1 forces the 1611A micro-processor (A5U11) to increment through the complete address range of the ROM board (0000₁₆ to FFFF₁₆). This addresses all locations in ROM 0. The signature analyzer verifies the data contents of all locations in ROM 0. It also verifies proper operation of all 1611A micro-processor address lines.

SIGNATURE ANALYSIS PROCEDURE NO. 1.

- a. Set 1611A LINE switch to off position.

- b. Remove A6, A7, A8, A9, and A10 boards from 1611A.
- c. Reinstall A10 board on extender board A14.
- d. Ground A5U3 pin 6 and A5U11 pin 6.
- e. Connect signature analyzer probes to the following circuit points:

START A5U11, pin 36

STOP A5U11, pin 38

CLOCK A5U11, pin 17

GND A5TP (GND)
- f. Set signature analyzer controls as follows:

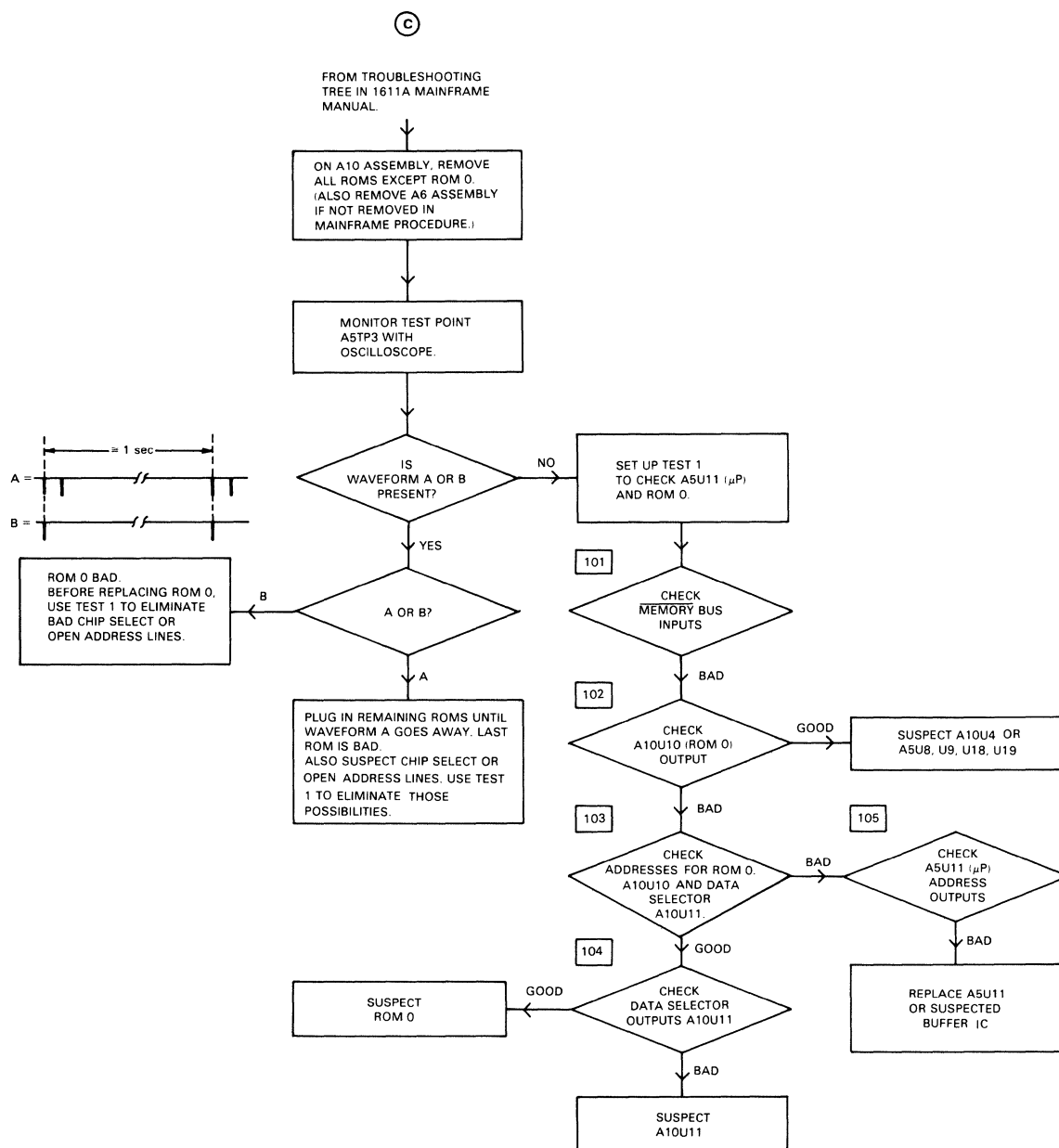
START 

STOP 

CLOCK 
- g. Set 1611A LINE switch to on position.
- h. Verify that signatures called out in troubleshooting tree match the following table.

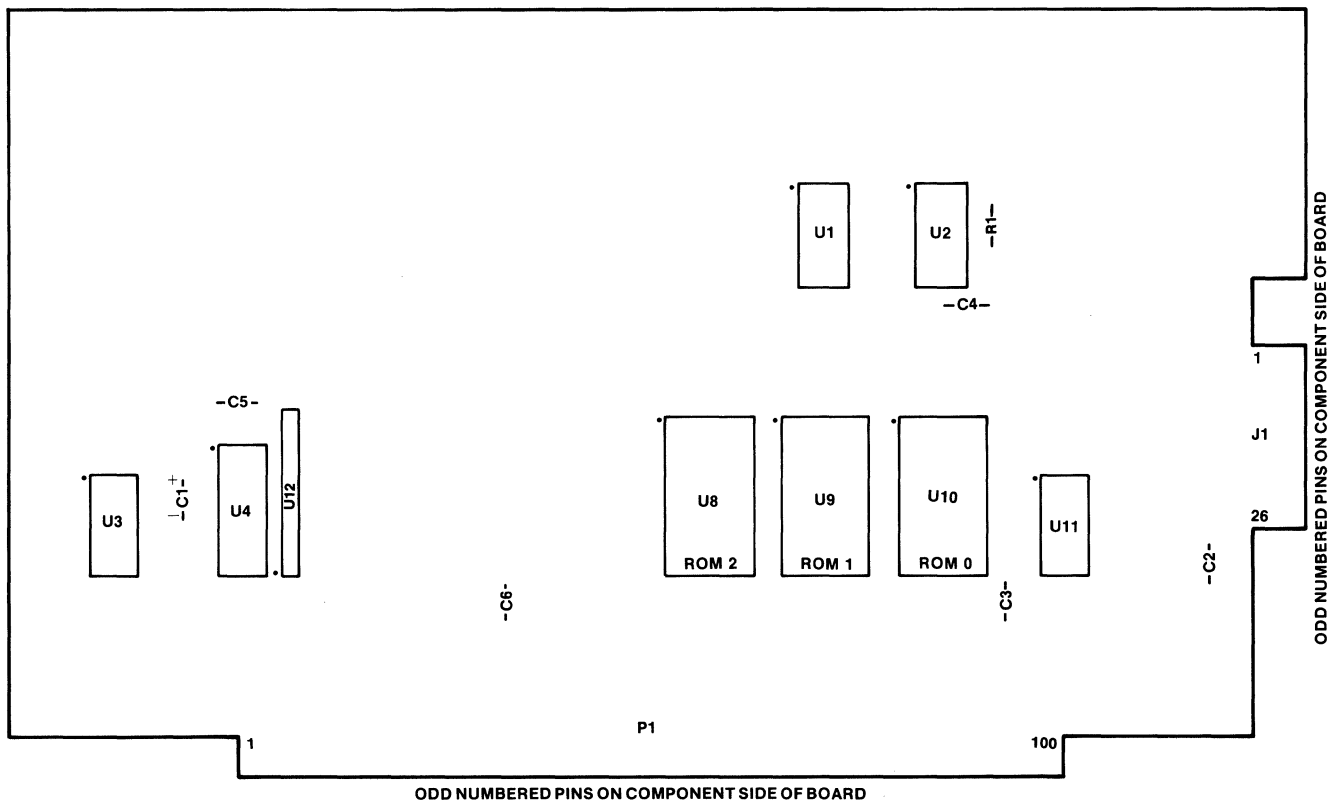
MEASUREMENT NUMBER	TEST POINTS	SIGNATURES	
	A10 ROM boards 01611-66532 and 01611-66570	A10 board 01611-66532	A10 board 01611-66570
101	V _H A5U8, pin 5 A5U8, pin 1 A5U8, pin 9 A5U8, pin 13 A5U9, pin 5 A5U9, pin 1 A5U9, pin 9 A5U9, pin 13	P254 A8PF UPAF AOUA 314F C583 600F A220 CH06	P254 U85F 131F 31CH C160 P5FP H35A 9HU9 5124
102	A10U10, pin 9 A10U10, pin 10 A10U10, pin 11 A10U10, pin 13 A10U10, pin 14 A10U10, pin 15 A10U10, pin 16 A10U10, pin 17	4AC8 1FU8 42AP H318 57H7 8258 4074 5U52	1A08 U148 H39P 5334 079A 310P 7UAH C370
	A10 ROM boards 01611-66532 01611-66570	A10 board 01611-66532	A10 board 01611-66570

MEASUREMENT NUMBER	TEST POINTS	SIGNATURES	
103	A10U10, pin 8 A10U10, pin 7 A10U10, pin 6 A10U10, pin 5 A10U10, pin 4 A10U10, pin 3 A10U10, pin 2 A10U10, pin 1 A10U10, pin 23 A10U10, pin 22 A10U11, pin 1 A10U11, pin 2 A10U11, pin 3	5P33 FA11 3HUA 12U0 C7A5 46HC 65CA 8AUC 9241 1U5P AAHU U665 82P6	5P33 FA11 3HUA 12U0 C7A5 46HC 65CA 8AUC 9241 1U5P U665 826P 0000
104	A10U11, pin 15 A10U11, pin 14 A10U11, pin 13 A10U11, pin 12 A10U11, pin 11	879F 6CC3 931U 1U0A 4A78	0P7C 6P41 1A4A not used not used
	A10 ROM boards 01611-66532 and 01611-66570	A10 ROM boards 01611-66532 01611-66570	
105	A5U21C, pin 7 A5U21C, pin 6 A5U21B, pin 5 A5U21B, pin 4 A5U21A, pin 3 A5U21A, pin 2 A5U21D, pin 9 A5U21D, pin 10 A5U21E, pin 11 A5U21E, pin 12 A5U12E, pin 11 A5U12E, pin 12 A5U12F, pin 13 A5U12F, pin 14 A5U12C, pin 7 A5U12C, pin 6 A5U12B, pin 5 A5U12B, pin 4 A5U2B, pin 6 A5U2B, pin 5 A5U2A, pin 3 A5U2A, pin 2 A5U12A, pin 3 A5U12A, pin 2 A5U2C, pin 8 A5U2C, pin 9	5P33 5P33 FA11 FA11 3HUA 3HUA 12U0 12U0 C7A5 C7A5 65CA 65CA 8ACU 8ACU 9241 9241 1U5P 1U5P AAHU AAHU U665 U665 826P 826P V _{LP} V _{LP}	
V _{LP} = 0000			



ROM Test Troubleshooting Tree

Figure 8-4. Service Sheet 4, ROM Board A10 (Sheet 1 of 3)



A65 ROM Board A10 Parts Identification (01611-66570)

Figure 8-4. Service Sheet 4, ROM Board A10 (Sheet 2 of 3)

